Upgrade of the MDC-DAQ system

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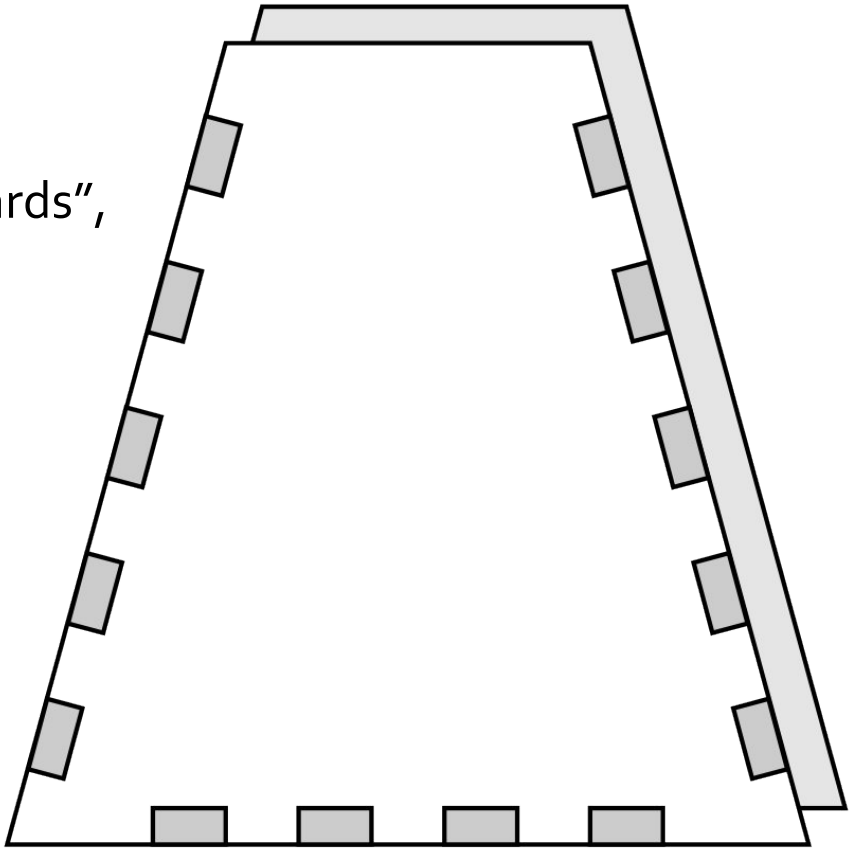
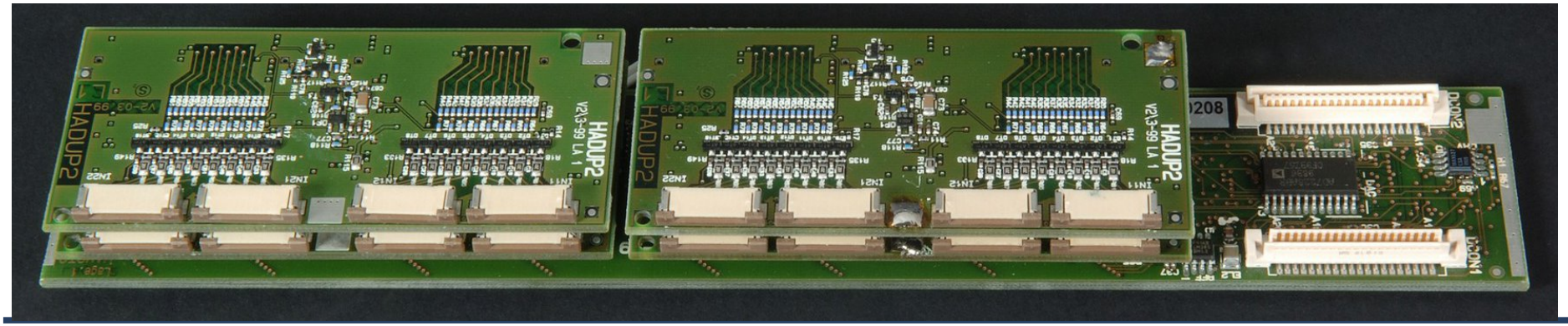
MDC DAQ – Front End Electronics (FEE): Motherboards

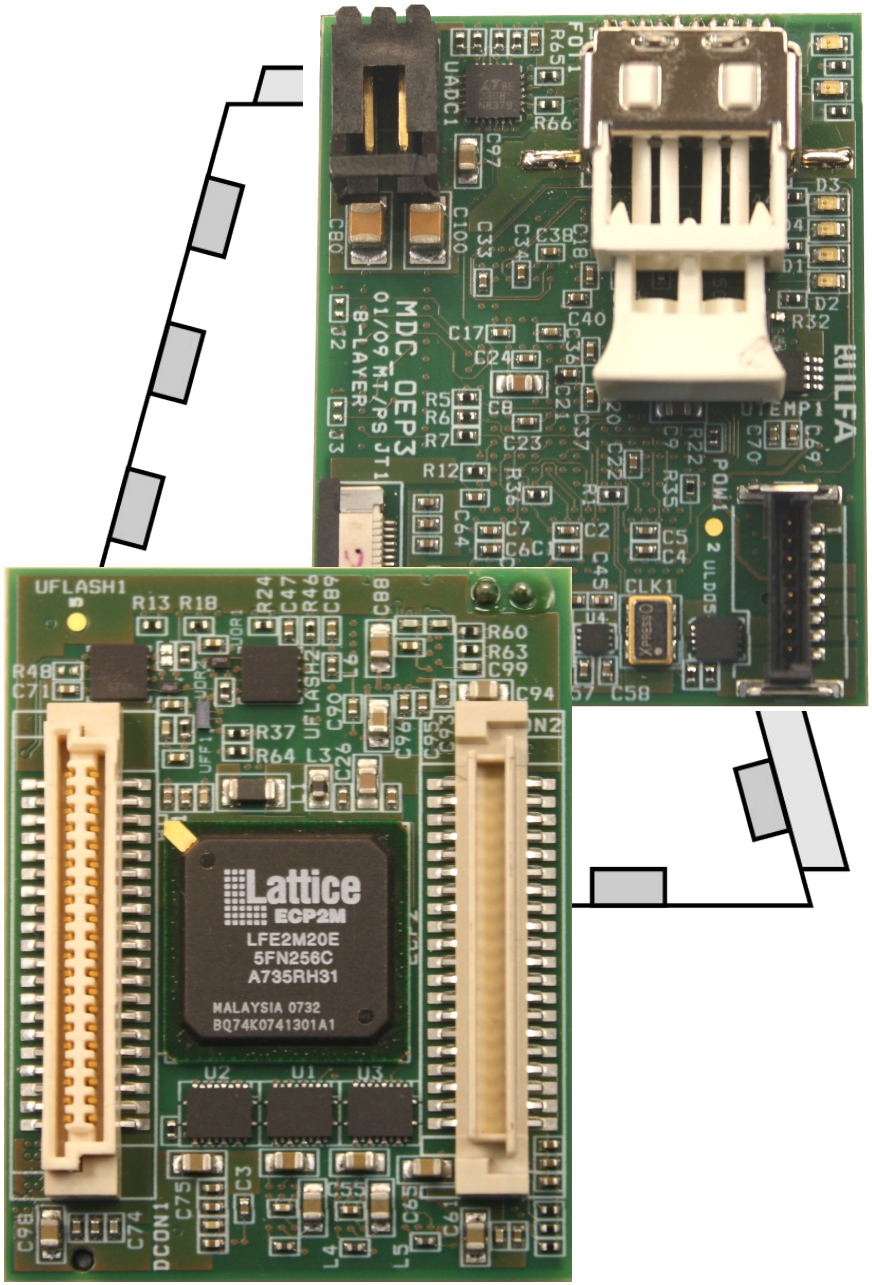
- Each chamber is equipped with 16 "motherboards", each carryingTDCs and
- "daughterboards" with amplifiers
- Amplifies analog signals from sense wires
- 64 or 96 channels
- Time resolution 500 ps



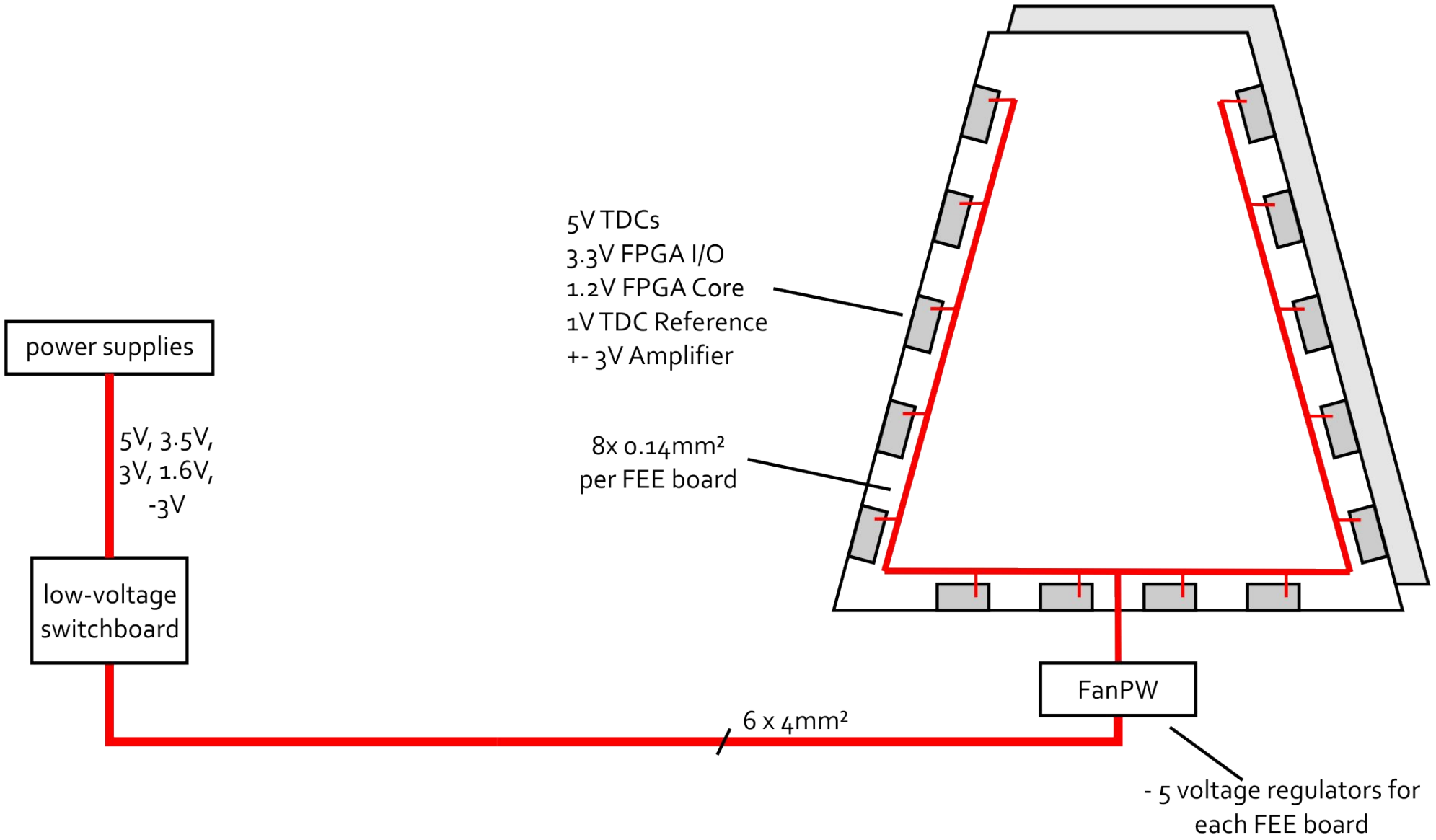


MDC DAQ – Front End Electronics: OEP

- FPGA configures, controls and read data from motherboards
- Sends data to PCs / storage (Eventbuilder)
- Motherboard and OEP need many voltages: 5V, 3.3V, 1.2V, 1V, +3V, -3V
- All voltages are monitored, 4 are regulated on-board
- 2 Flash ROMs to store different FPGA designs
- Temperature sensor
- 250 Mbit/s optical transceiver
- … and all on a board measuring just 4 x 5 cm²!



MDC DAQ: Power distribution



MDC DAQ: Power distribution - Components

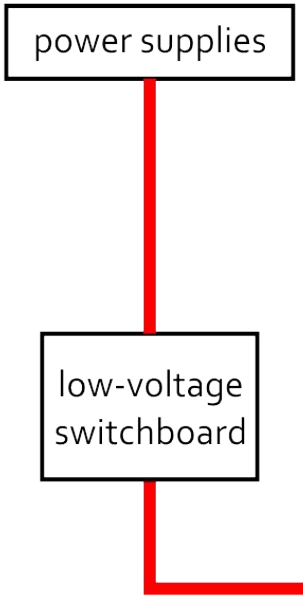
power supplies

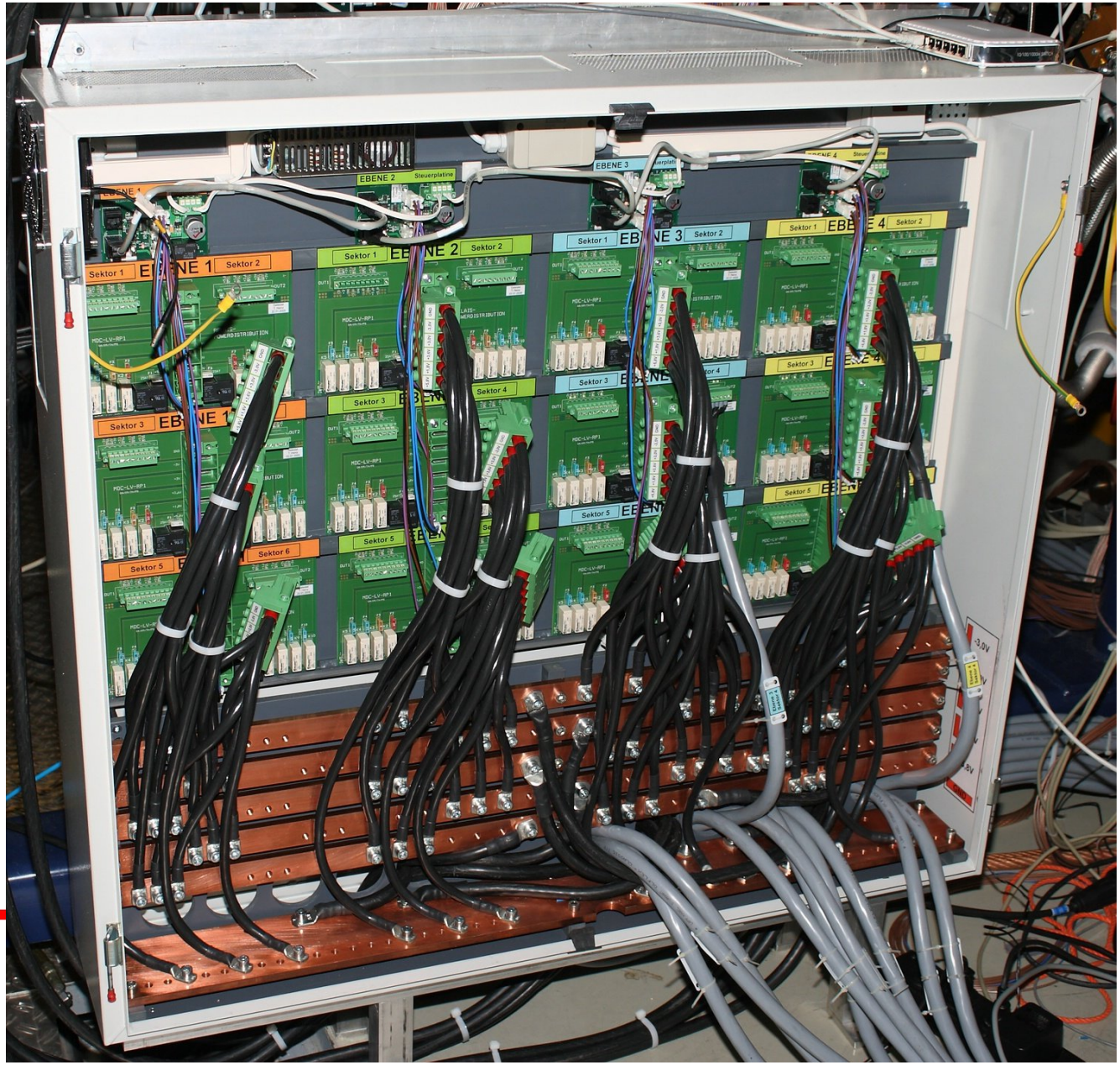
low-voltage switchboard

FanPW

MDC DAQ: Power distribution - Components

120 relais & fuses
800 A total current
5 voltages between -3 and 5V





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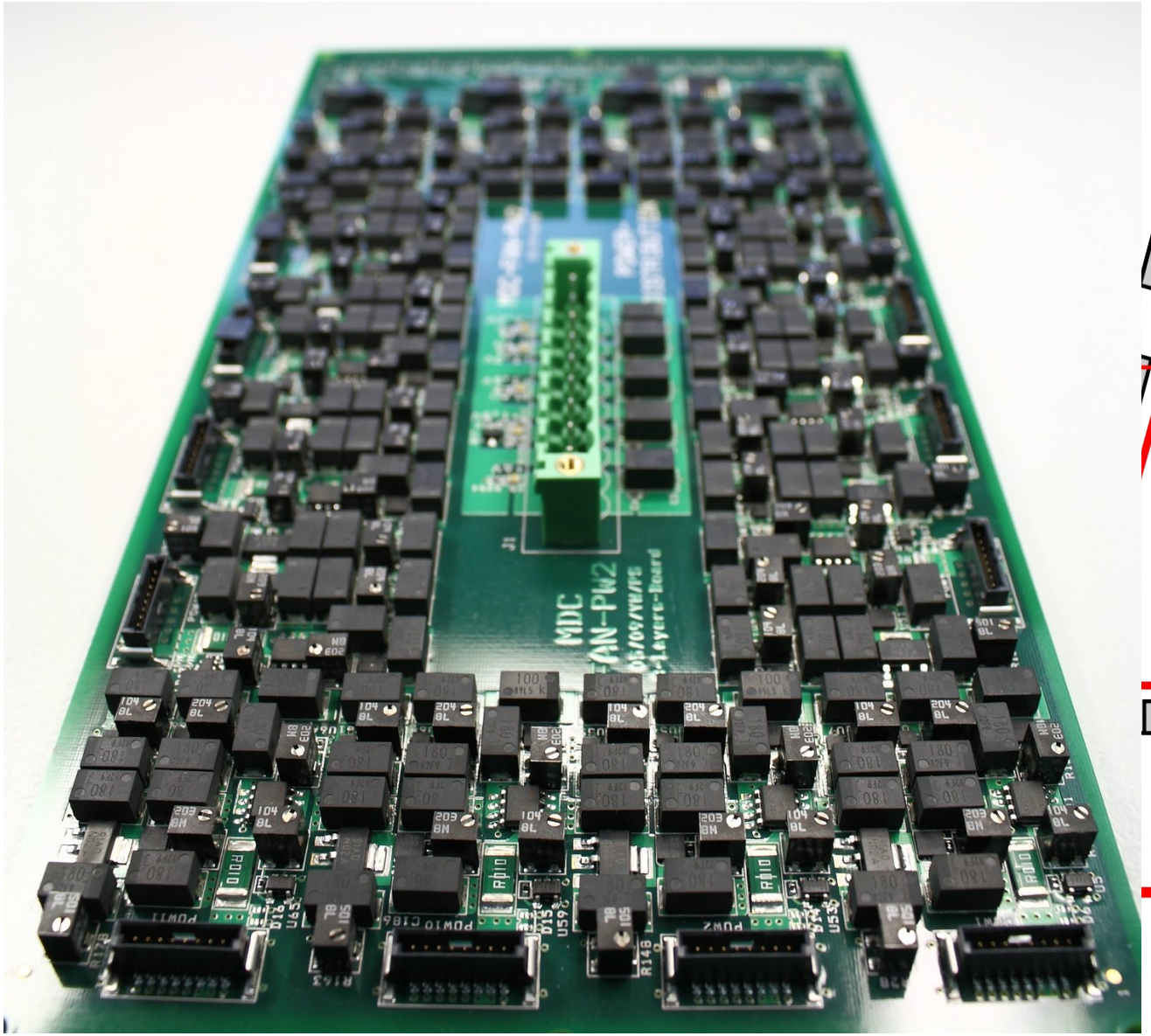
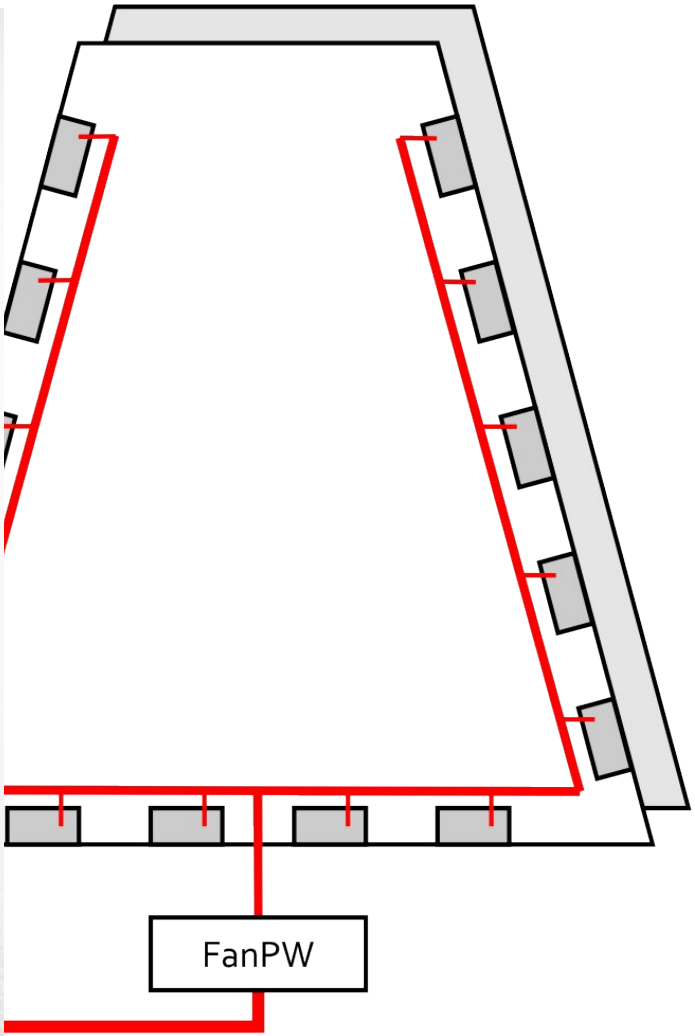
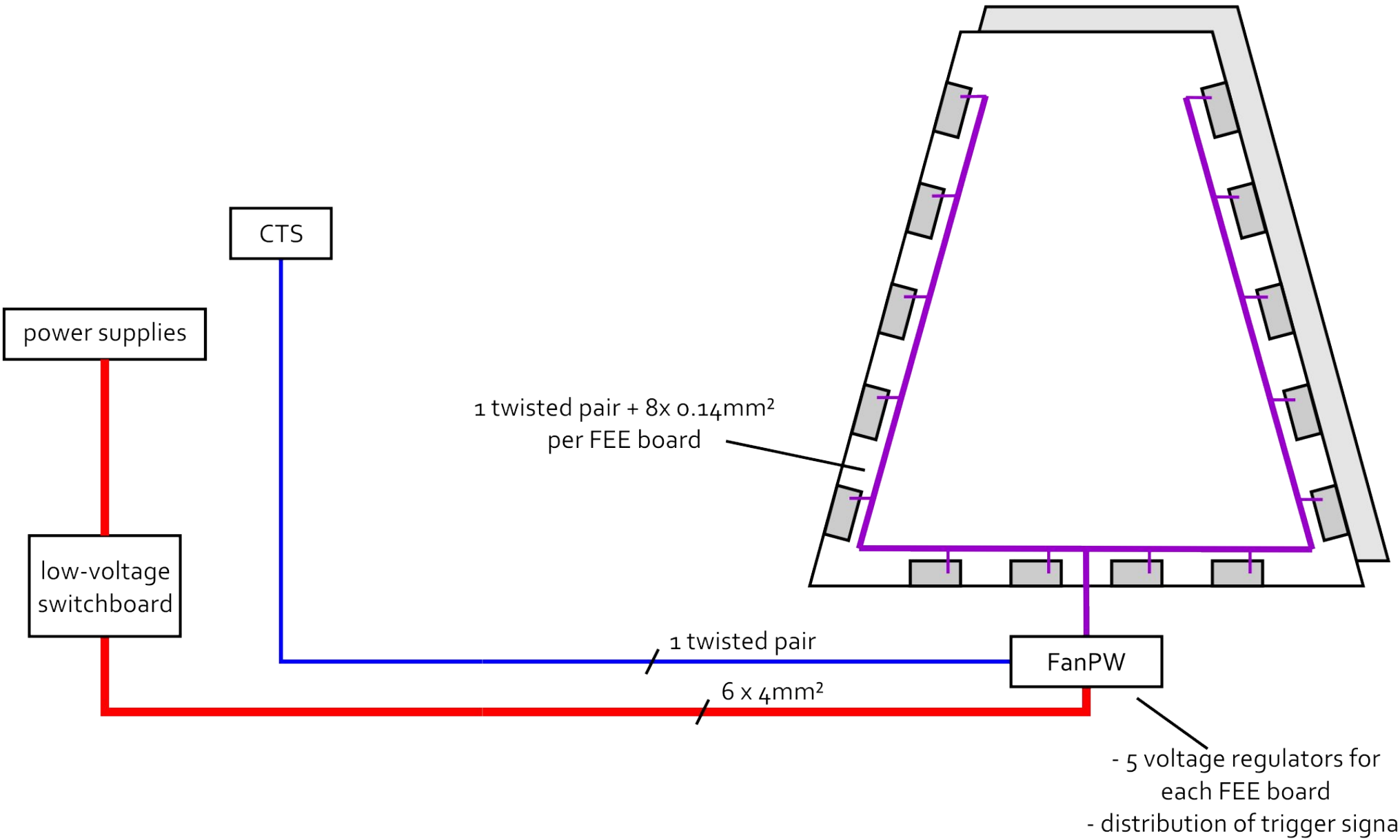


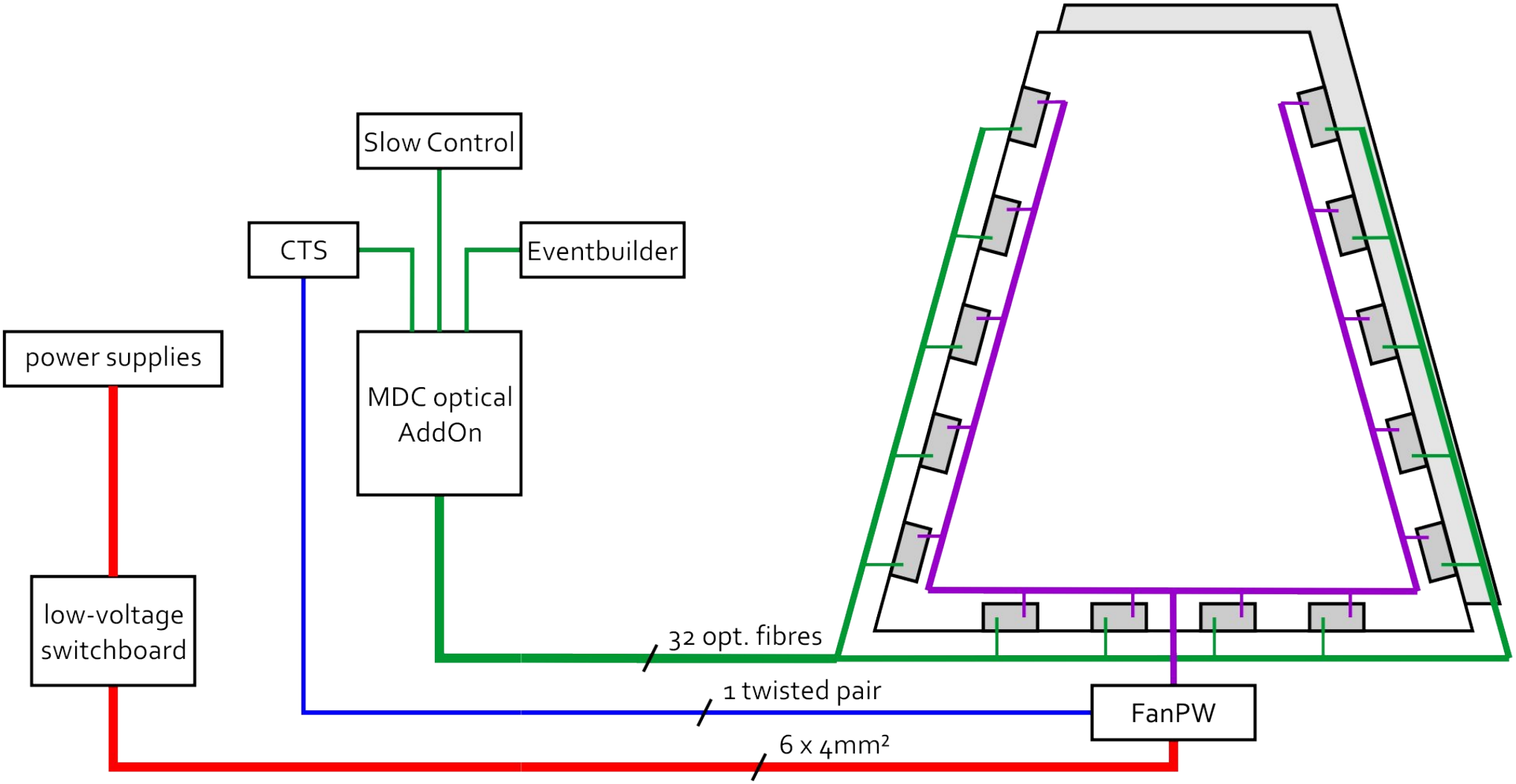


108 voltage regulators
35 A total current

MDC DAQ: Trigger Distribution



MDC DAQ: Optical Network



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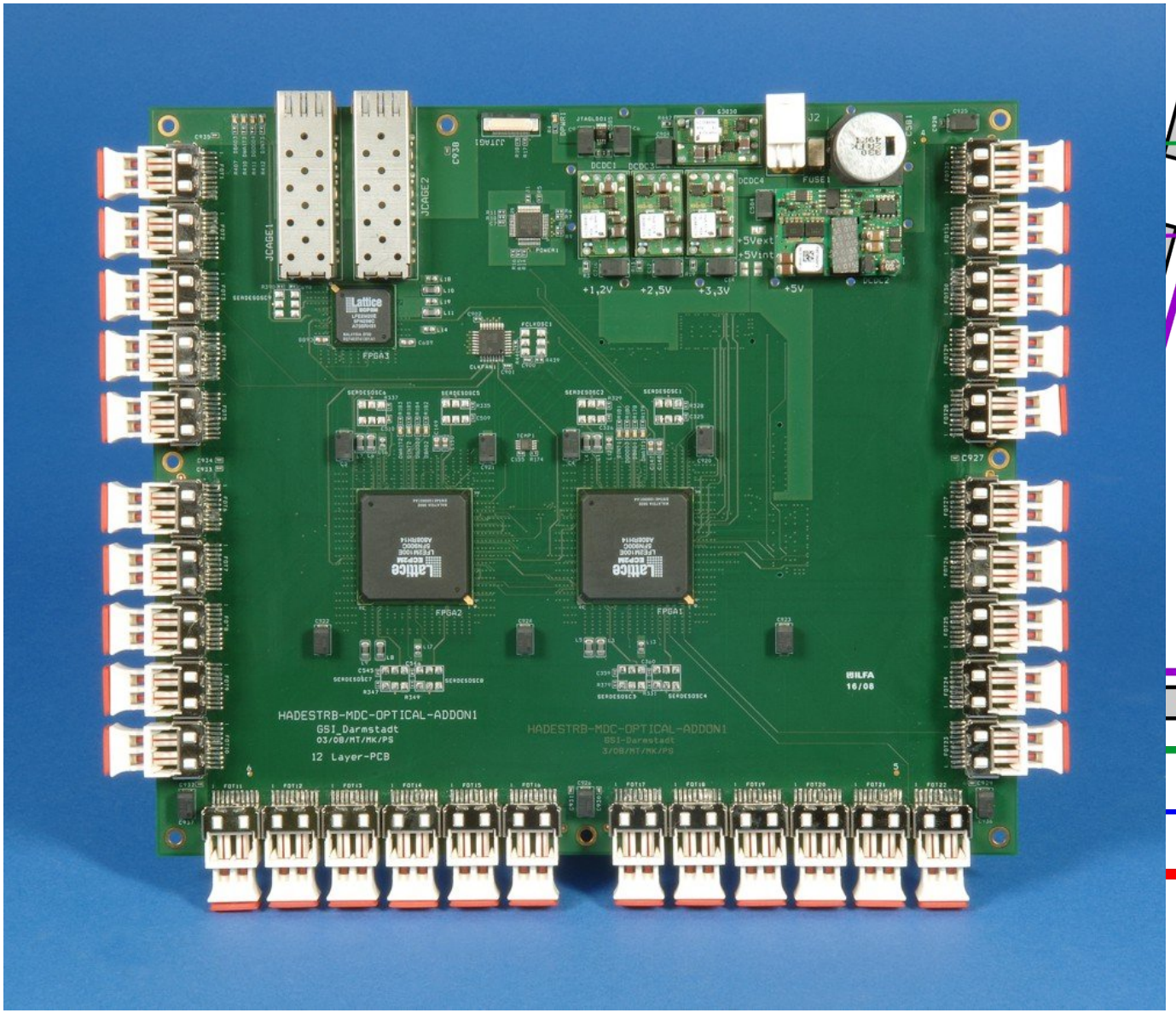

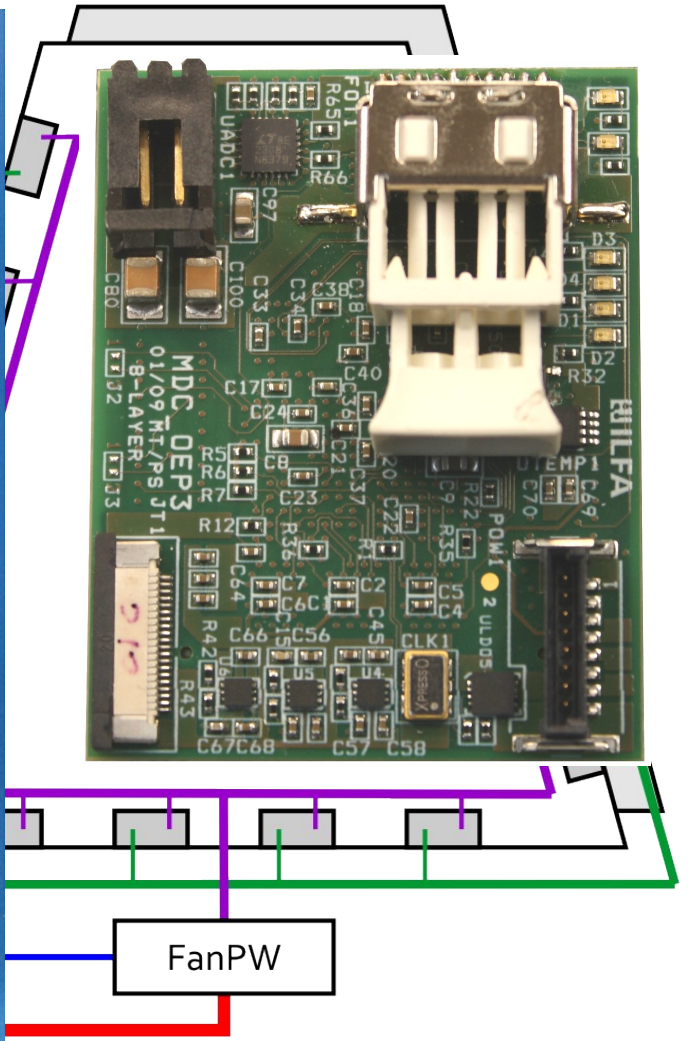

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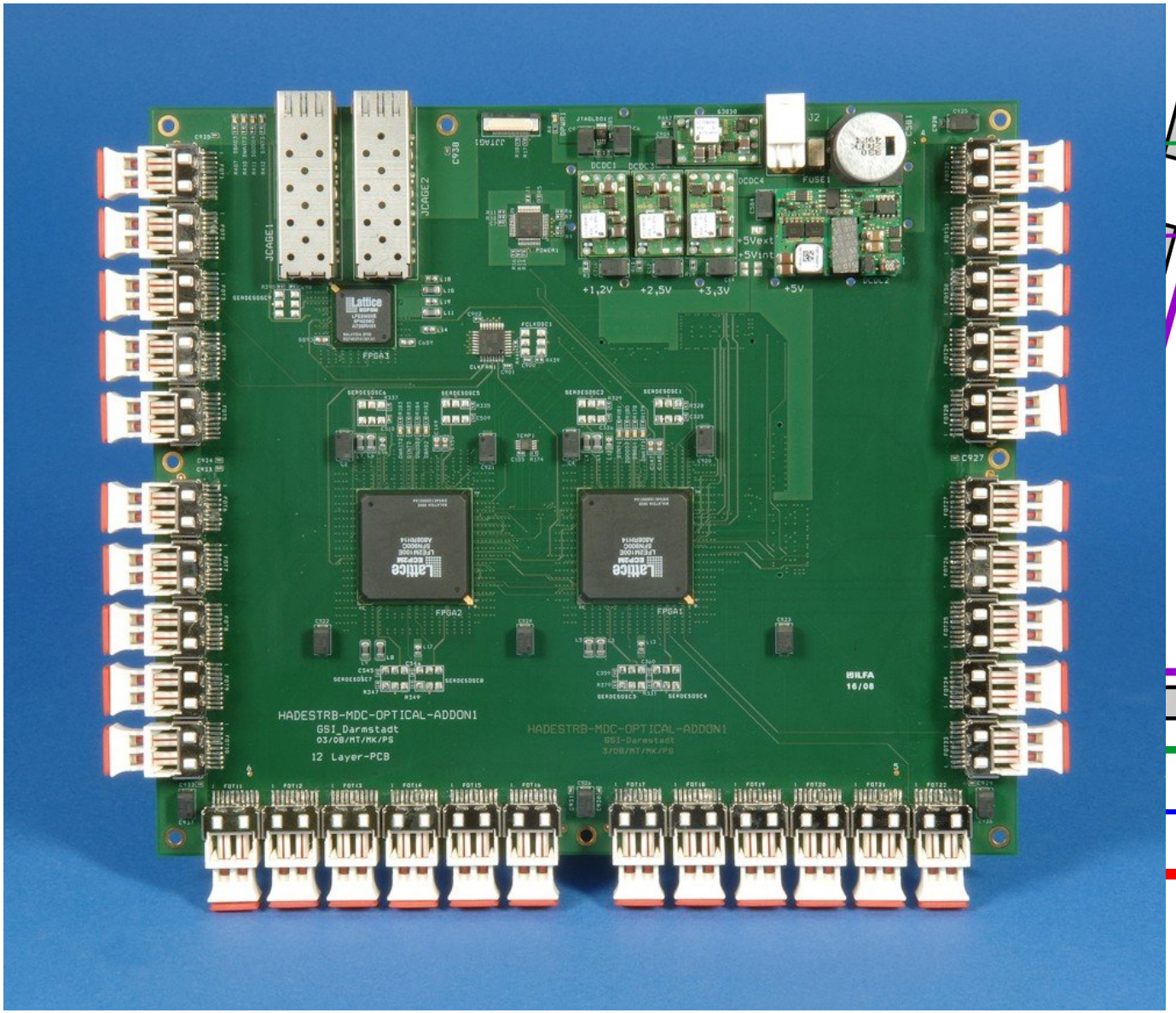

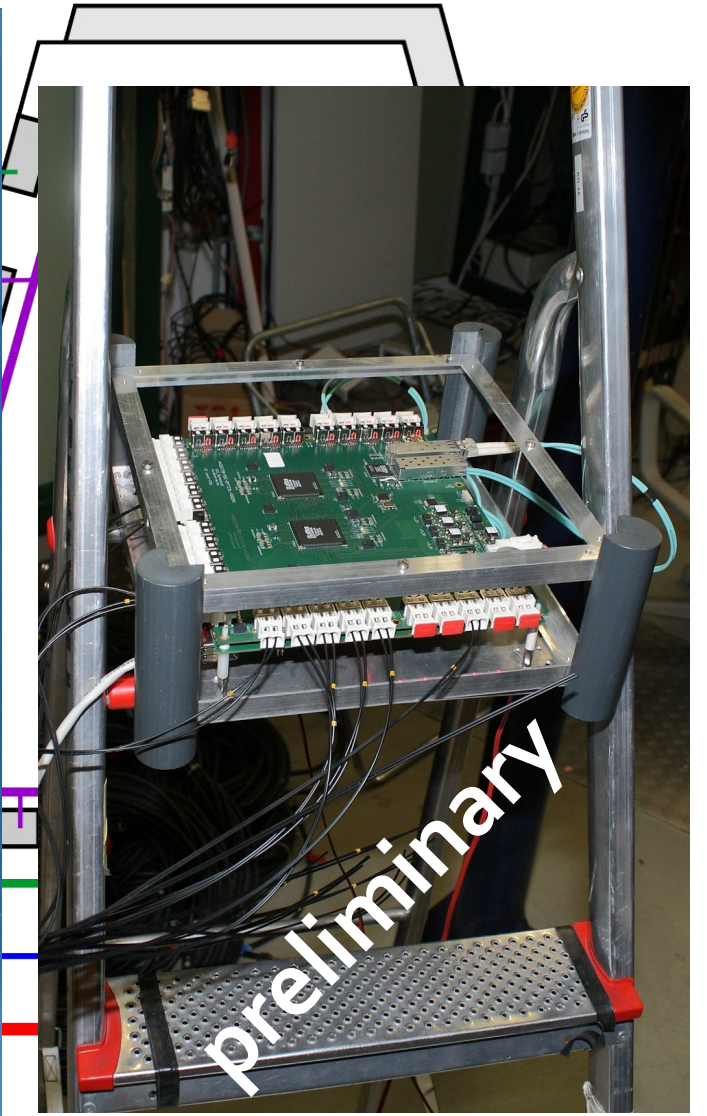

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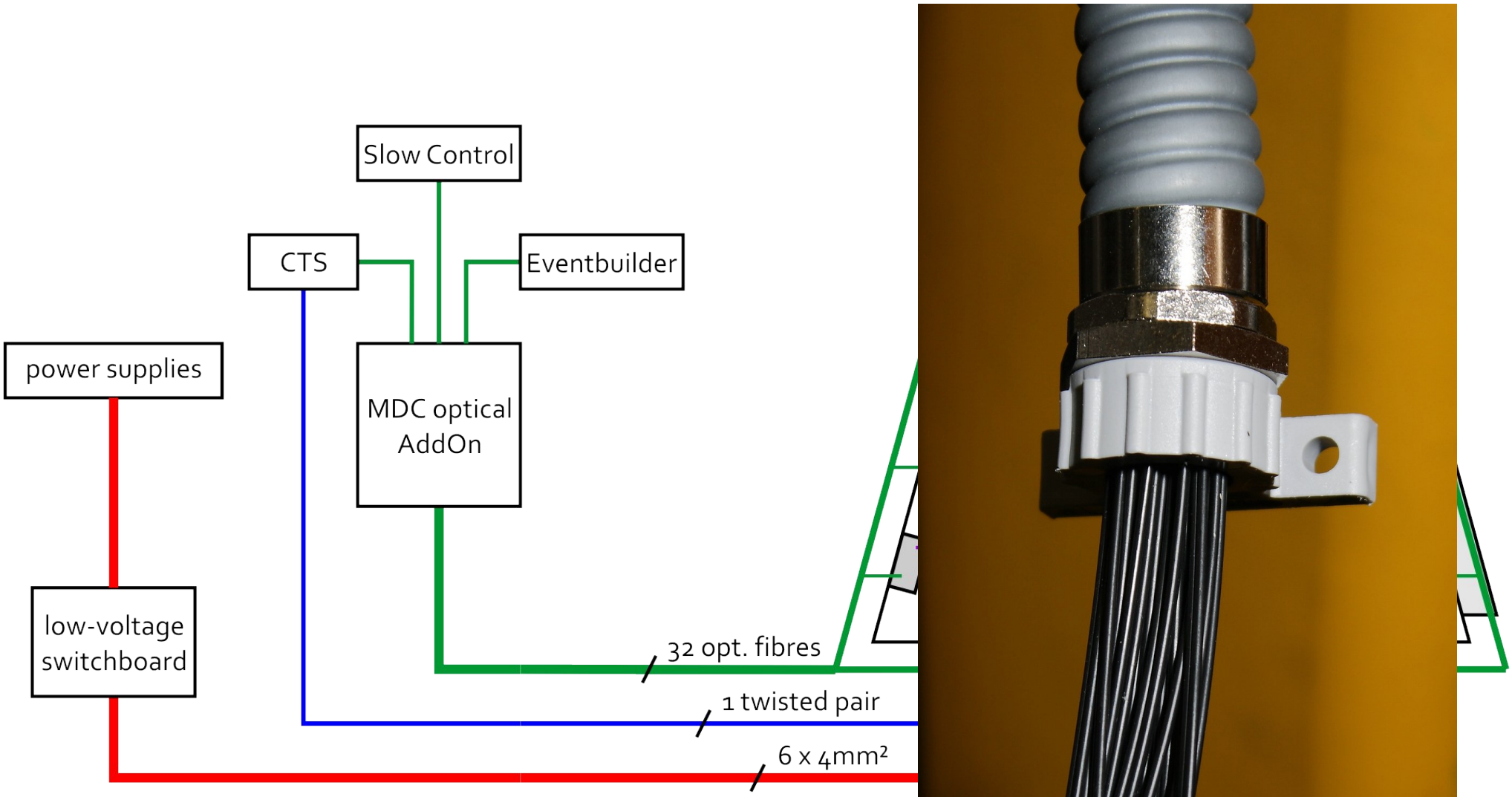

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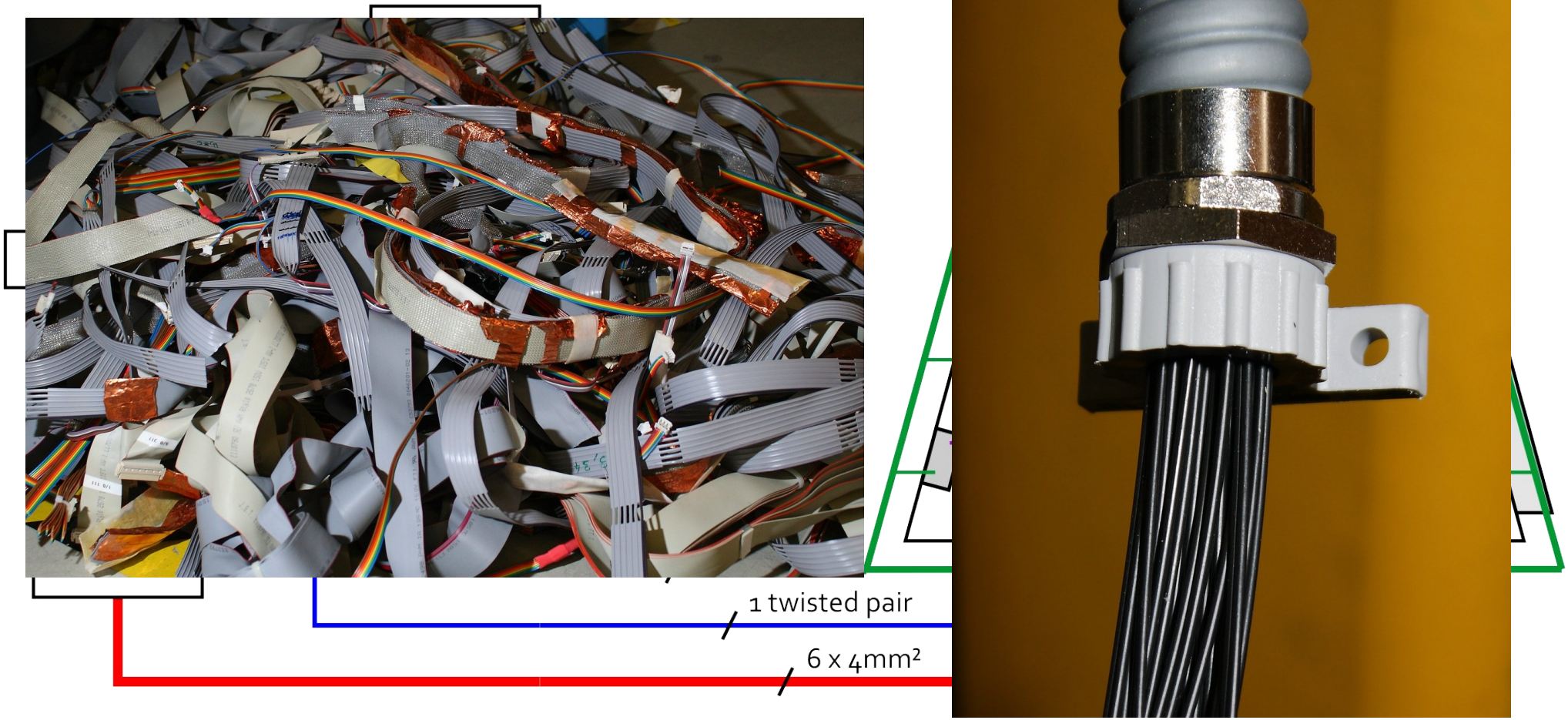
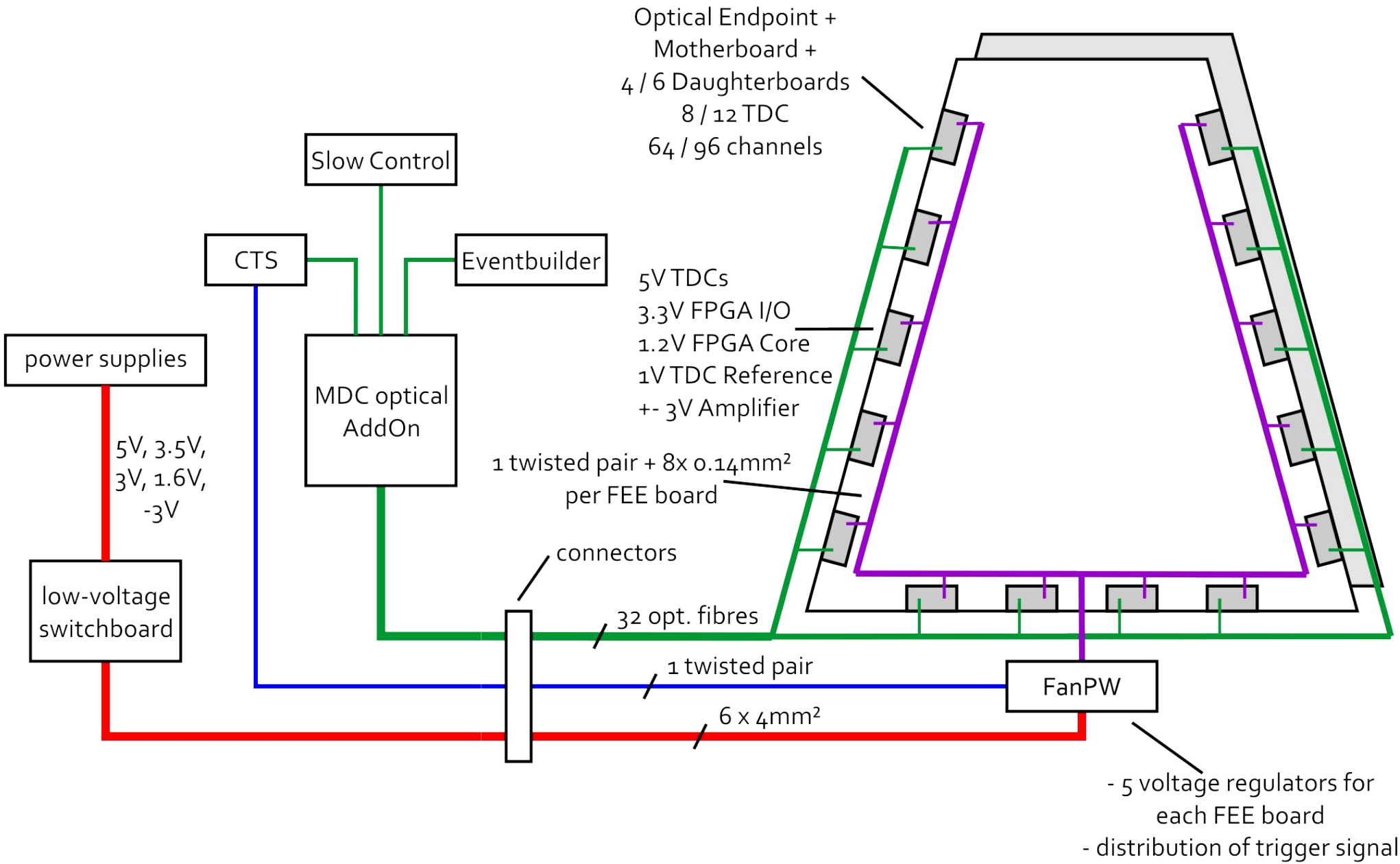


MDC DAQ: Optical Network - Components



MDC DAQ: Current Status

- Power Supplies: installed
- Low-voltage Switchbox: installed
- Cable from swtichbox to chambers: installed
- Optical cables from AddOn mounting point to chambers: installed
- Optical Endpoints: mass production running, 40 ready
- MDC AddOns: 4 prototypes available, mass production: end of year
- Readout tests & noise measurement with one half chamber: successful
- All chambers equipped with new readout: ~ december

MDC DAQ: Software - libtrbnet

- C-Library to access all Boards inside DAQ optical network
- Allows to manually test all request types on TrbNet
- Main purpose: Slow Control / Debugging / Monitoring
- Split into TrbNet-library, FPGA-connection library & high-level software
  - Easy to implement in own code

```
Commands:
   r <trbaddress> <register>                  -> read register
   w <trbaddress> <register> <data>           -> write register
   rm <trbaddress> <register> <size> <mode>   -> read register-memory
   wm <trbaddress> <register> <mode> <file>   -> write to register-memory from ASCII-file
   i <trbaddress>                             -> read unique ID
   s <uid> <endpoint> <trbaddress>            -> set trb-address
   T <input> <type> <random> <info> <number>  -> trigger by slowcontrol
   I <type> <random> <info> <number>          -> read IPU data slowcontrol
   f <channel>                                -> flush FIFO of channel
   R <register>                               -> read register of the FPGA
   W <register> <value>                       -> write to register of the FPGA
```

```
> trbcmd i ffff
0xee000001e43c17c1  0x01
0x8e000001fc533228  0x01
```

MDC DAQ: Software - trbflash

- Programming flash ROMs (FPGA design) on all OEPs and RICH ADCM via trbnet
- Much faster than conventional programming via JTAG
- Can programm all 400 boards at once
- Essential tool – some boards are not accessible after mounting

```
> trbflash program 0xfffd mdc_oepb_golden_alpha3.bit
Found 2 Endpoint(s) of type MDC
NAME: mdc_oepb_golden_alpha3.bit
DATE: Mon Oct  5 11:23:25 2009
USER:
Start programming ImageFile 'mdc_oepb_golden_alpha3.bit'
You decided to reprogram the FlashRom(s) #1 of MDC, are you sure [N,y]: y
Programming Endpoint(s) @ Address 0xfffd
Symbols:
  E: Erasing
  P: Programming
  V: Verifying
  X: Failed (see logfile 'trbflash.log' for details)
  @: Success
  .: Skipped

Block: 0 1 2 3 4 5 6 7 8 9 A B C D E F
0      @ @ @ @ @ @ @ @ @ @ @ @ . . . .
1      . . . . . . . . . . . . . . . @

Success
```

Also available: readout software, compatible to Eventbuilder standard
Under development: Direct readout via Ethernet to Eventbuilder