TrbNet – The new trigger and readout network for HADES

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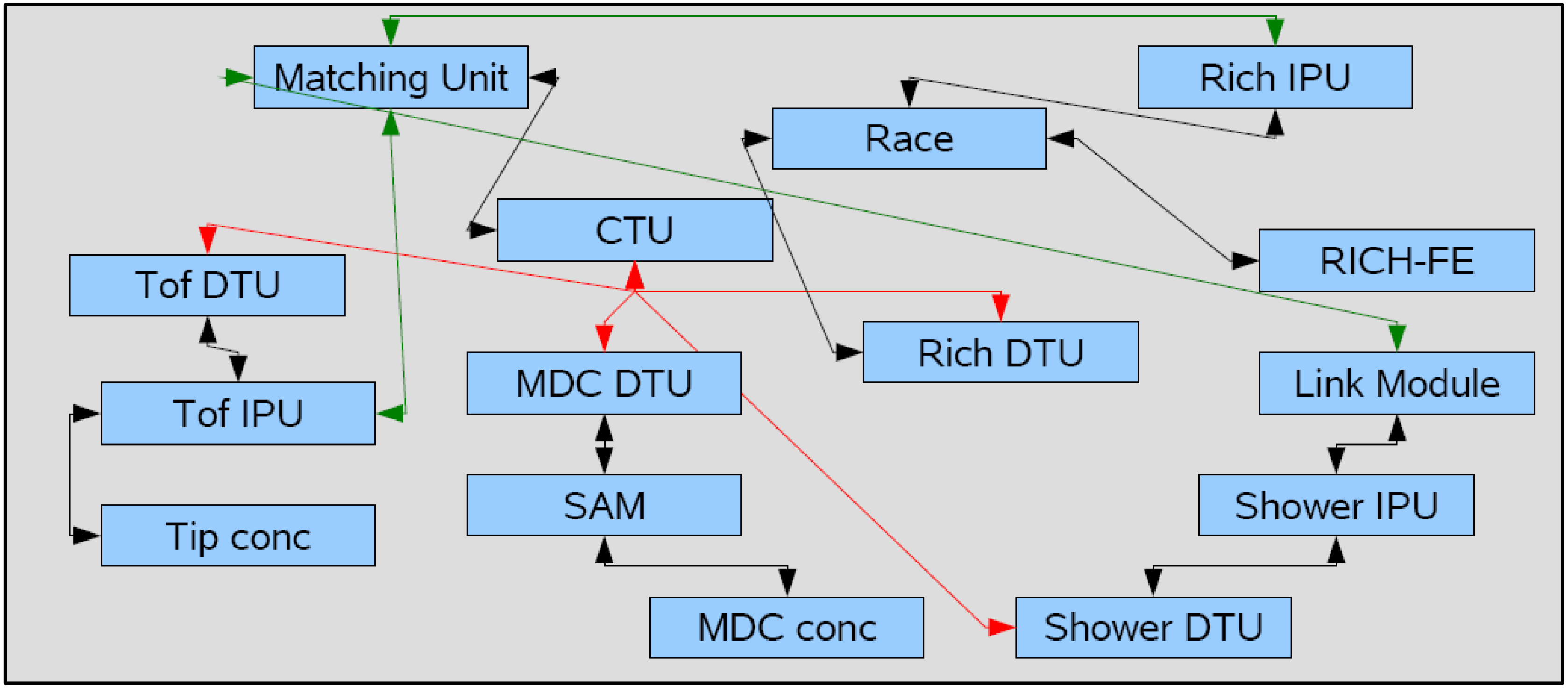
Outline

- Why and how the old trigger network is replaced
- Brief view of the network protocol
- Features of the new network protocol
- Performance measurements

Requirements – Why do we need a new network?

- too many different hardware types and protocols involved
- no feedback from modules
- length oriented data transfers
    - ↪ no handshake protocol, risk of buffer overflows
- bulky cables: hard to handle & introducing noise

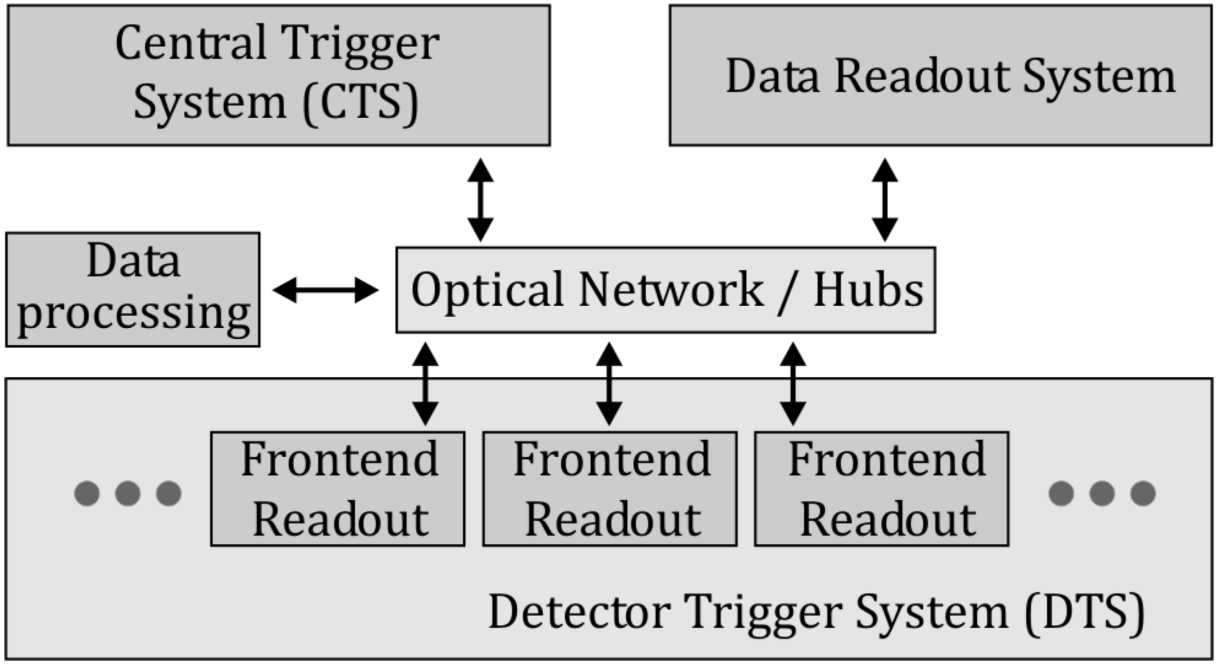


Requirements – What features are needed?

- One network protocol for all connections including FEE readout
  - ↪ Easy to use & maintain
- One common network for triggers, data & slow control
  - ↪ Fast data transmission > 1 Gbit/s for data
  - ↪ Low latency < 5 μs for triggers
- Network transparent for applications
  - ↪ No application has to bother with network protocol
- Protocol adaptable to all hardware setups
  - ↪ Small boards need low hardware consumption
  - ↪ High performance network nodes
- Modular code design to easily change parts of logic
  - ↪ Network medium can be chosen for each link individually
  - ↪ Code is reusable in different configurations

Network Setup

- Optical networks and hubs connect all parts
  - ↪ Fast connections & negligible influence on detector
- Most boards are based on programmable logic (FPGAs)
  - ↪ Only a small number of different devices is used
- Processing algorithms can be applied to data during transport
  - ↪ Placement of IPU algorithms in FPGAs



Data Format

Challenge: fast triggers & data on the same network

- Network is divided into channels

  ↪ Transfers can run in „parallel"

  ↪ Each channel uses independent resources despite network media

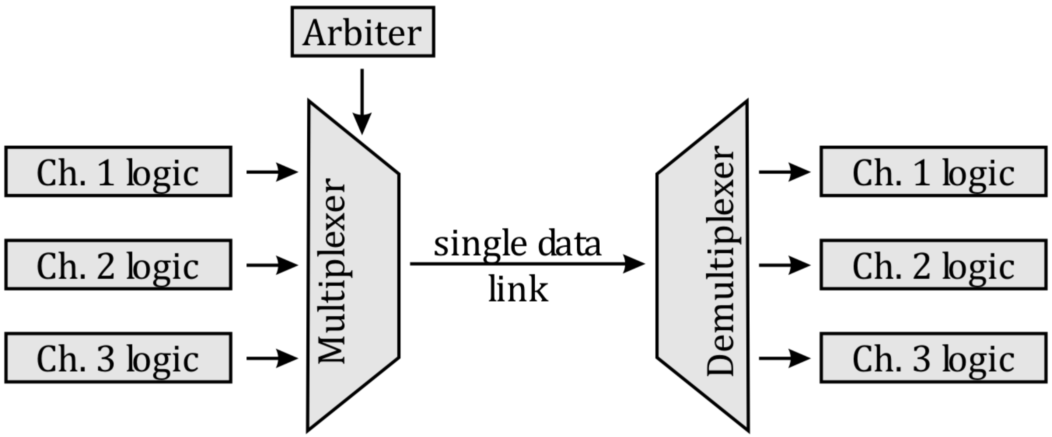
- Four channels will be used:

  LVL1 trigger

  IPU data

  LVL2 trigger / data read-out

  Slow control



- All data is transported as small packets with 64 bit

  ↪ Channels can be switched very fast

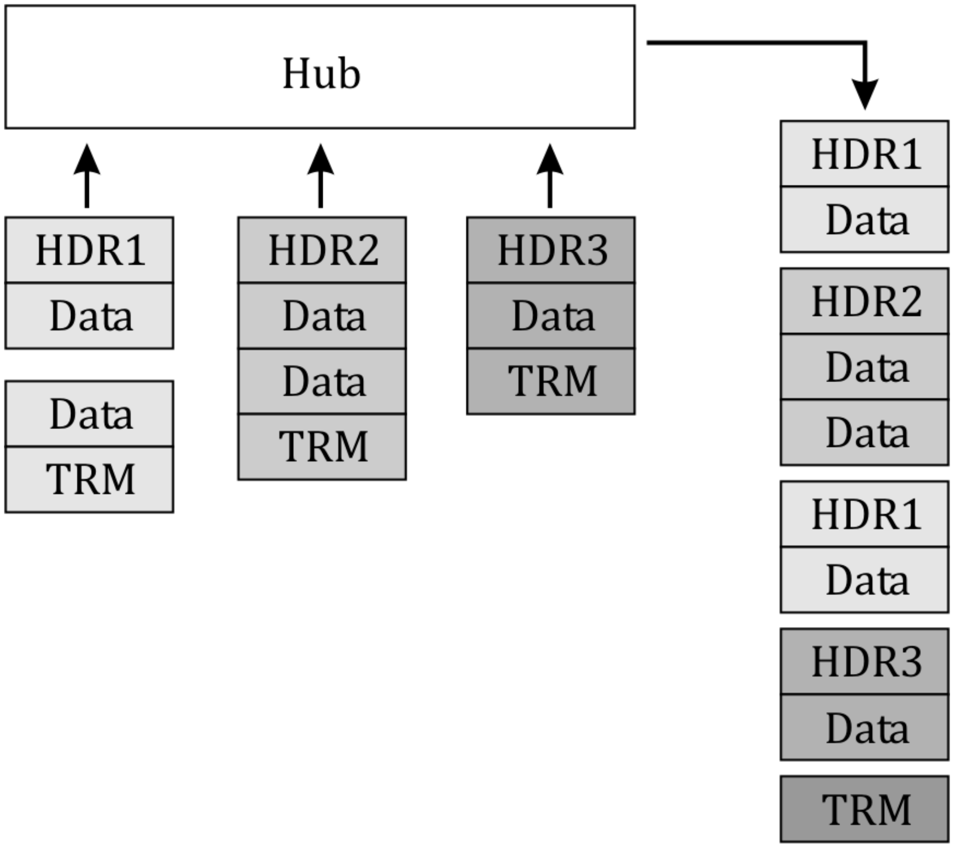
63-56	55-51	50-48	47 – 0
reserved	Channel / Path	Packet Type	Datawords

Features I: Slow Control

- All devices are connected to the same network
  - ↪ Slow control can be done from one terminal
- Every board has standardized status registers
  - ↪ Easy implementation of an overall status screen
- Multiple boards can be addressed simultaneously
  - ↪ One command to get the status of the whole electronics
- Detector specific control with additional registers
- Each board is identifiable by a network address and on-board ID
- Hubs can switch off individual ports
  - ↪ Exclude detectors with malfunctions from trigger distribution

Features II: Data Merging

- Many responses to a transfer are a common case for the network
  - ↪ All boards answer with a busy release packet after a trigger
  - ↪ Front end electronics send their data after a readout request
- Data from different endpoints is merged into one data stream inside hubs
  - ↪ This is the first step of **event building**
- Terminations (busy release) are merged into one packet
  - ↪ CTS gets one packet back that shows the detector is ready to accept the next trigger



Event Data Format: Example

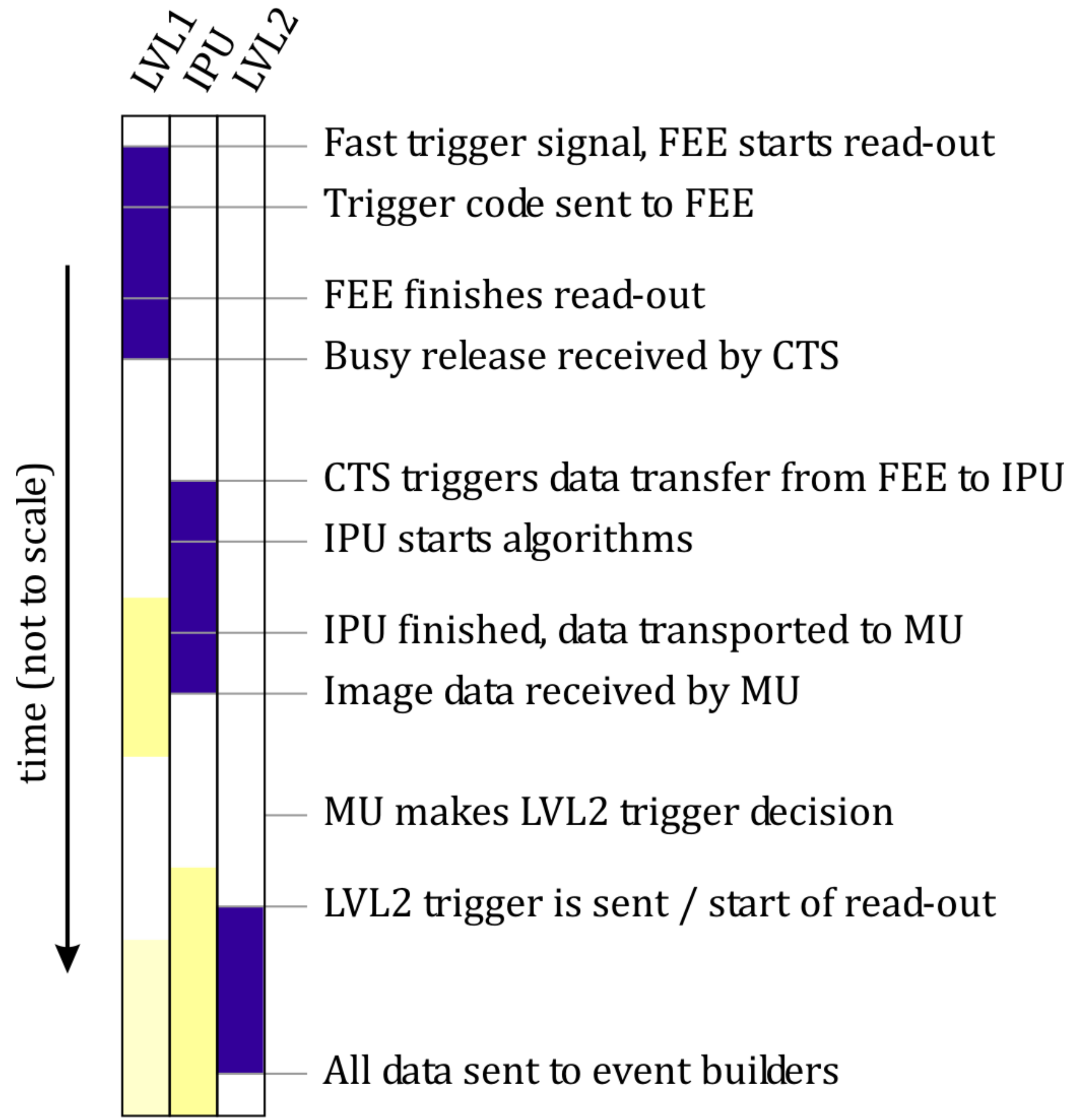
Channel number
Packet type

Request from CTS	0031	f009	ffff	0018
	0030	abcd	abcd	abcd
	0033	0000	0000	0018
Reply from FEE	0039	f00a	f009	0018
	0038	efef	efef	efef
	0039	f00b	f009	0018
	0038	efef	efef	efef
	0038	baba	baba	baba
	0039	f00a	f009	0018
	0038	baba	baba	baba
	0039	f00c	f009	0018
	0038	efef	efef	efef
	0038	baba	baba	baba
	003b	0001	0001	0018

Header & sender address
target address
Data
Termination

- All data is tagged with network address
  - ↪ No need for detector addresses in event format
- Redundant information can easily be extracted before writing data to tape

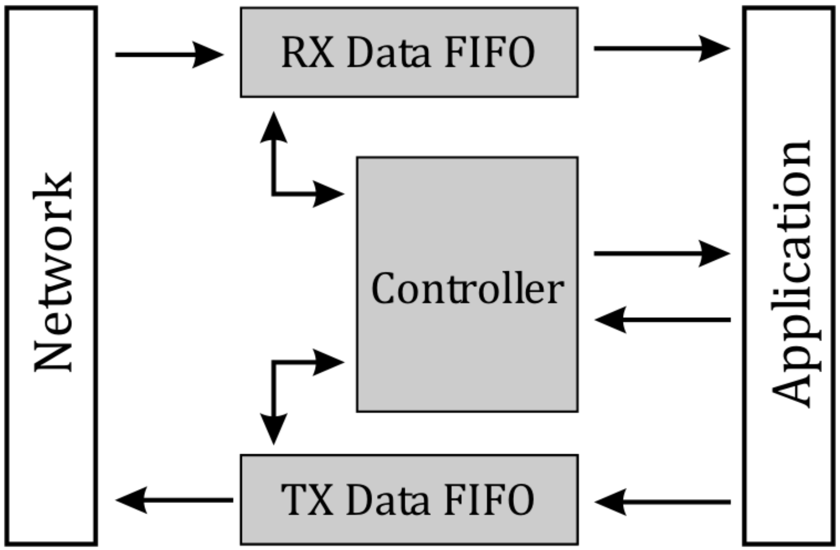
Trigger & Readout Process



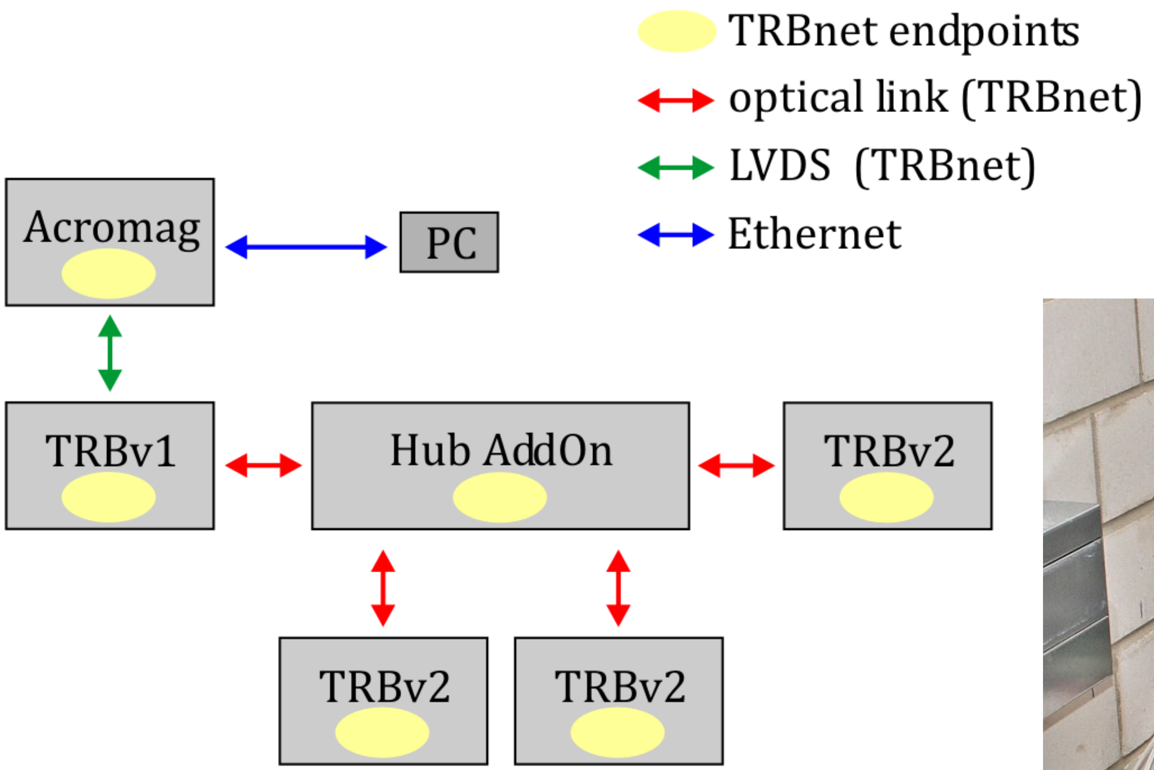
How to – Accessing the Network

- Sending / Receiving data is done by writing / reading data to / from a FIFO
- Additional ports for target address, type of transfer and error pattern
- Sending data is blocked during times where no transfer is allowed

  ↪ applications can not harm the network with erroneously sent data



Test Setup


TRBnet endpoints
optical link (TRBnet)
LVDS (TRBnet)
Ethernet
Acromag
PC
TRBv1
Hub AddOn
TRBv2
TRBv2
TRBv2

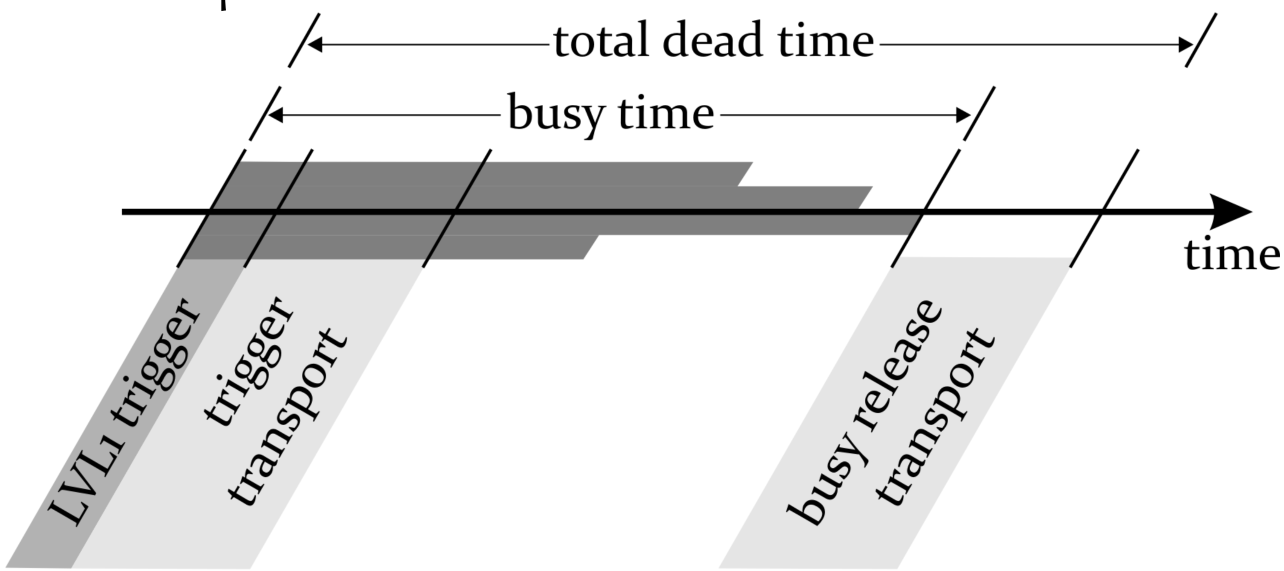
Latency – When will triggers arrive?

- longest connection: CTS to MDC FEE (optical)
  - ↪ CTS, 2 layers of hubs, TRB w. MDC concentrator, MDC frontend
  - ↪ 2 Xilinx, 4 Lattice FPGAs
  - ↪ 4 optical links, 1 LVDS connection

Packet Sizes	50	ns
Hub data handling	100	ns
10m optical fiber	60	ns
Xilinx Transmit & Receive	180	ns
Lattice Transmit & Receive	400	ns
Sum for one transfer	2100	ns

Trigger distribution and detector dead time

- LVL1 trigger signal is distributed using high speed cable
- Trigger code is sent over TrbNet
  - ↪ Arrives up to 2 μs after the fast trigger signal
- Release signal is sent by each detector when read out is finished
  - ↪ Transport of busy release adds 2 μs to the total detector dead time
- But: busy release can be sent earlier, if
  - ↪ … FEE can accept another trigger before having processed last one
  - ↪ … FEE busy time ends within 2 μs



Performance – How fast is it?

Bandwidth of optical links	100%	1.6	Gbit/s
Addressing & Locking	< 1%	0	Gbit/s
Packet Format	25%	0.4	Gbit/s
Handshake protocol	1%	0.02	Gbit/s
Detector data		1.18	Gbit/s

- 26% of bandwidth is used for protocol, 74% are available for data
- Other media available
  - ↪ LVDS via SCSI cable: cur. 200 Mbit/s
  - ↪ LVDS via AddOn connector: 1.6 Gbit/s
- Data rate of complete detector after LVL1 trigger: 3 Gbit/s
  - ↪ 1.2 Gbit/s are sufficient due to decentralized read out

Summary & Outlook

- Network protocol, network endpoints and hubs are almost finished
- Performance meets the requirements for high trigger rates
- Easy adaption to new devices / requirements is possible
- A lot of future extensions are possible
  - ↪ Higher network speeds
  - ↪ Switches with routing functions instead of hubs
- TrbNet is a universal network protocol, not for HADES only
  - ↪ Detector test setups with data readout from multiple boards
  - ↪ Free running, triggerless detectors (with modifications)

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Register Access: Example of a transfer

Channel number
Packet type

0031	f009	ffff	0018
0030	0080	0000	0000
0033	0000	0000	0018
0039	f00b	f009	0018
0038	0080	fff0	05c8
0039	f00a	f009	0018
0038	0080	1b20	16ce
0039	f006	f009	0018
0038	0080	0000	0000
0039	f007	f009	0018
0038	0080	0000	0000
003b	0001	0001	0010

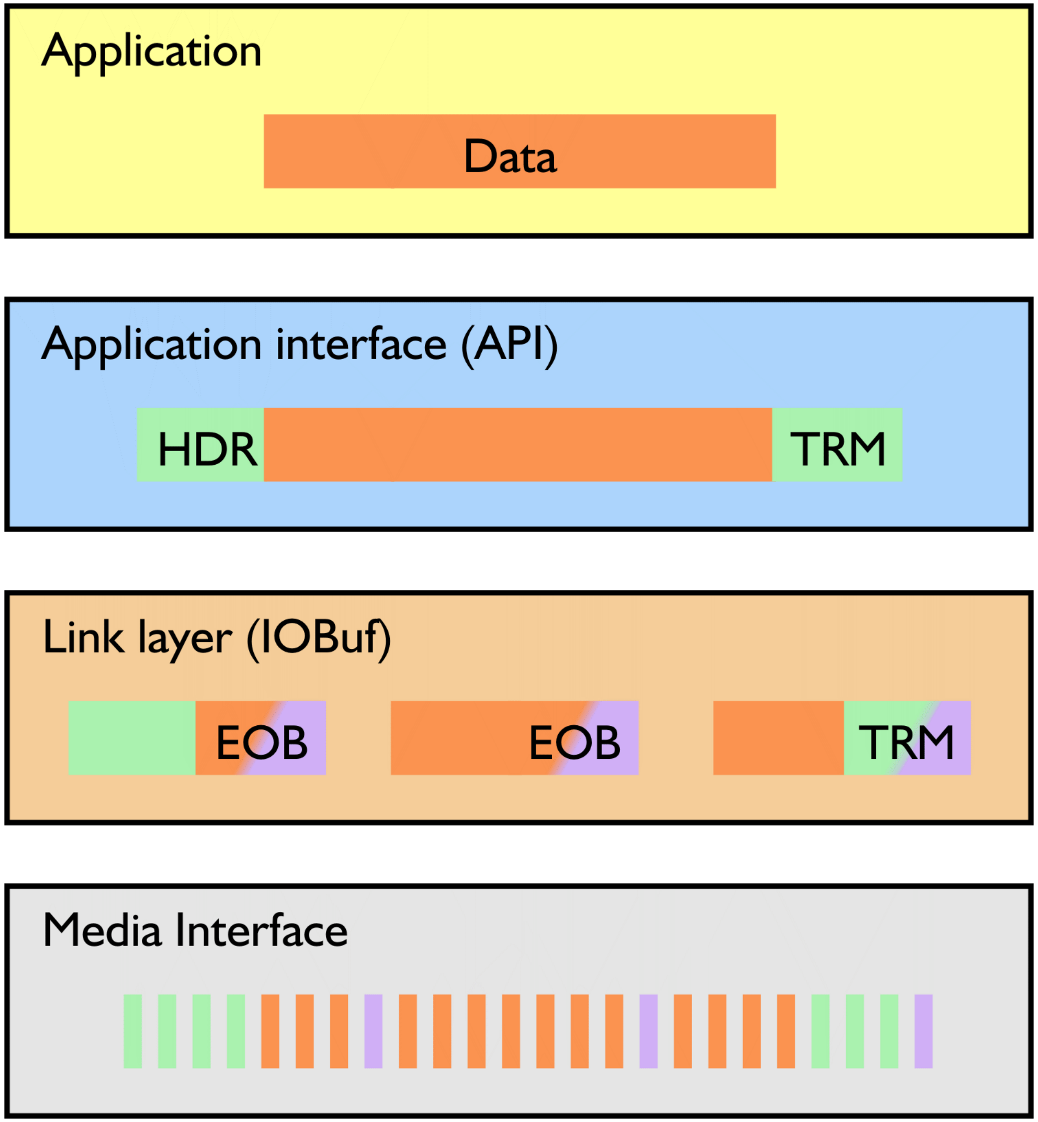
- Header & sender address
- target address
- Register data
- Termination
- Register address & operation

↪ Warning: Temperature sensor of board `F00B` is not responding.

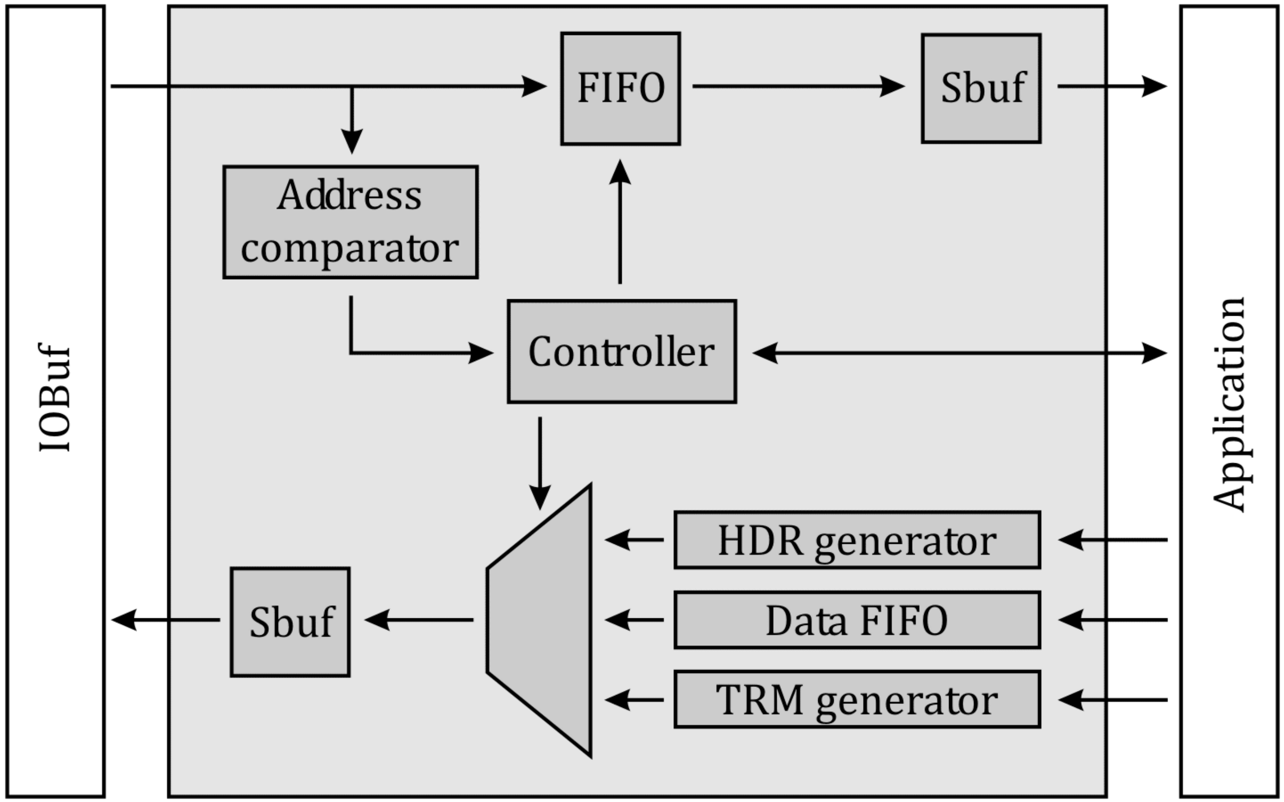
↪ Info: All temperatures are within normal range

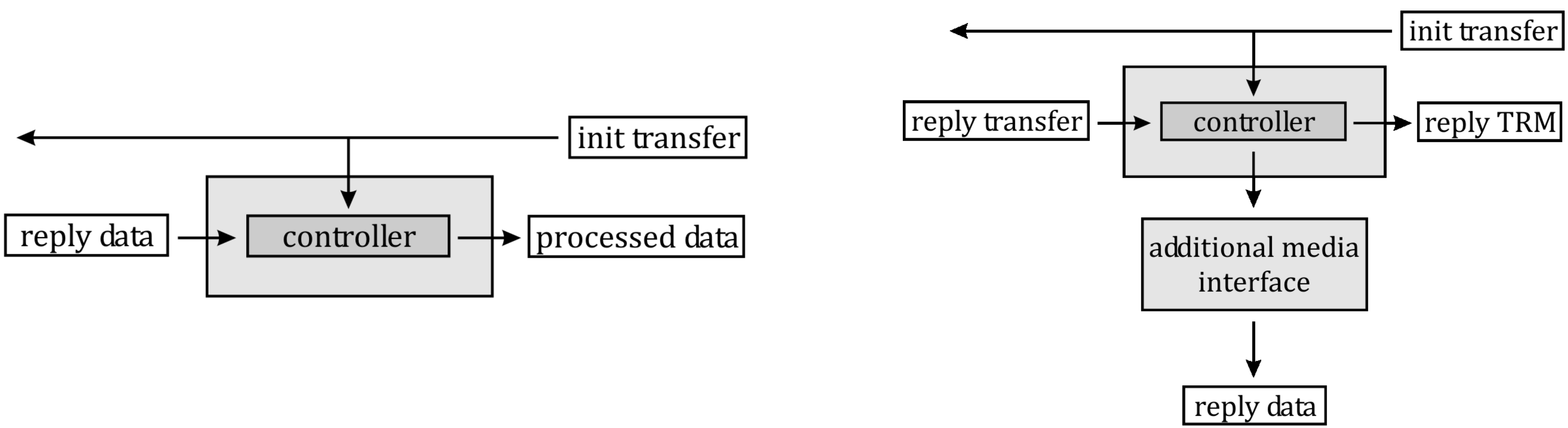
Network layers

- Interface between application and network is divided into 3 layers
- Application interface
  - ↪ adds header with addresses
  - ↪ controls access to network
- IOBuf
  - ↪ assures data integrity (CRC)
  - ↪ avoids data loss using buffers and handshake
- Media interface
  - ↪ prepares data for medium type
  - ↪ mostly optical links or LVDS

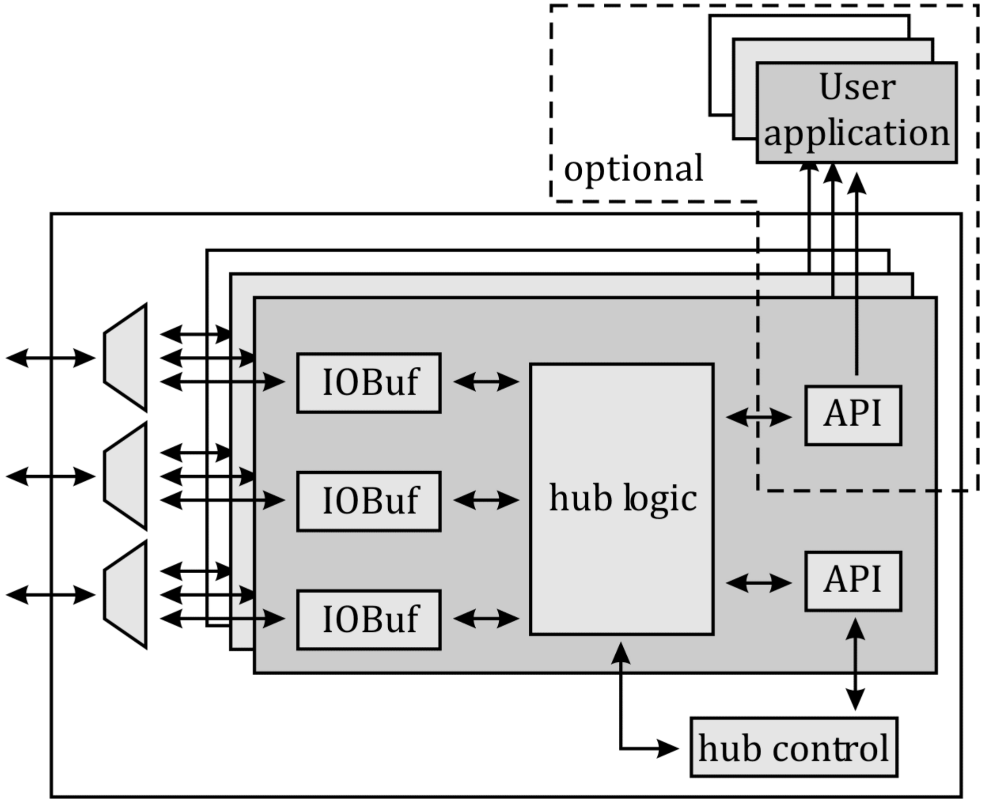


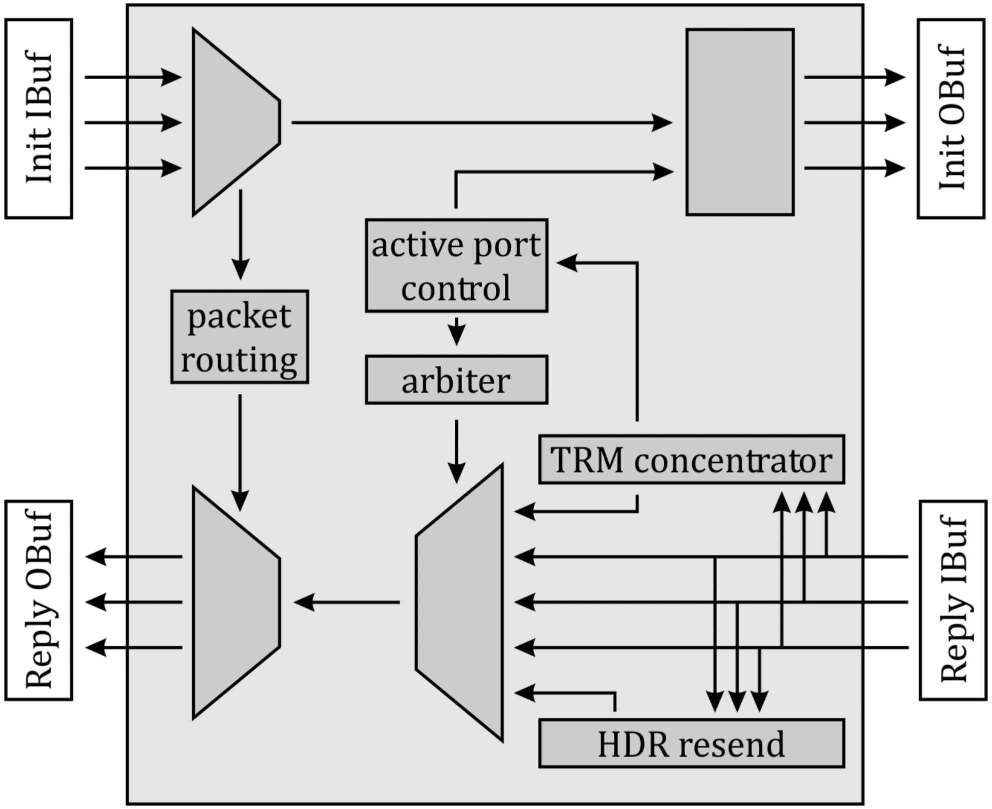
Application Interface / Streaming API



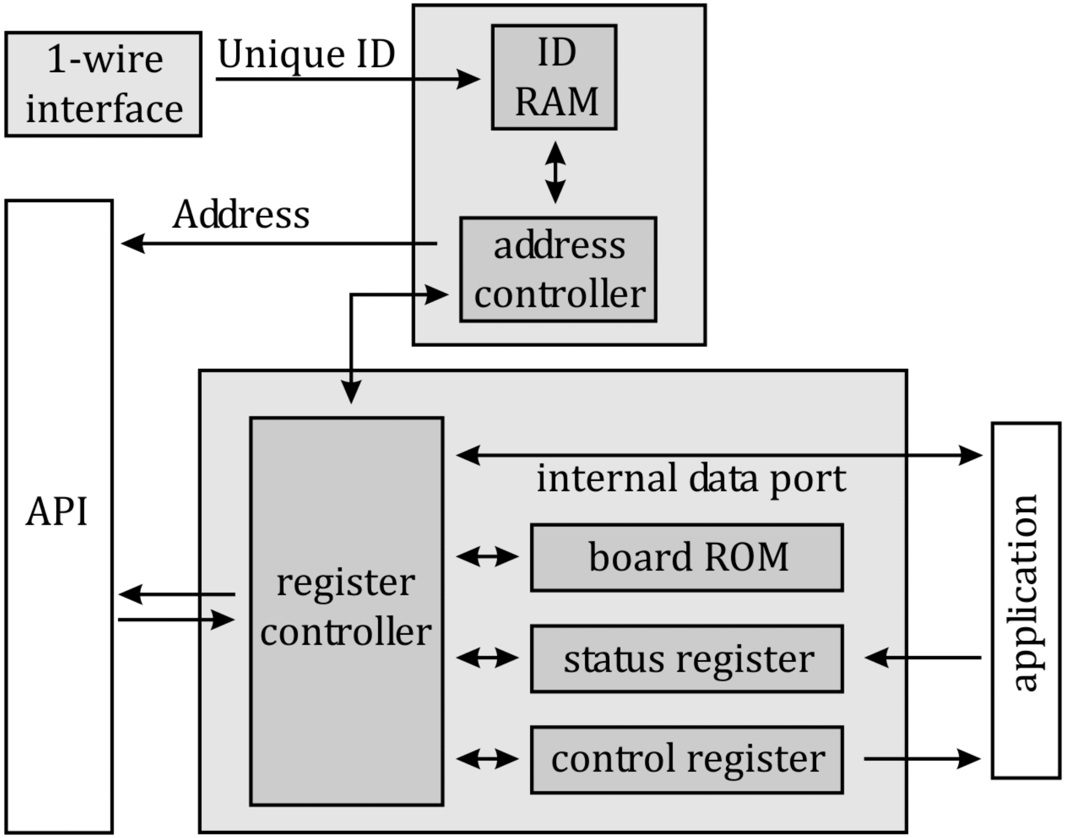


Hub

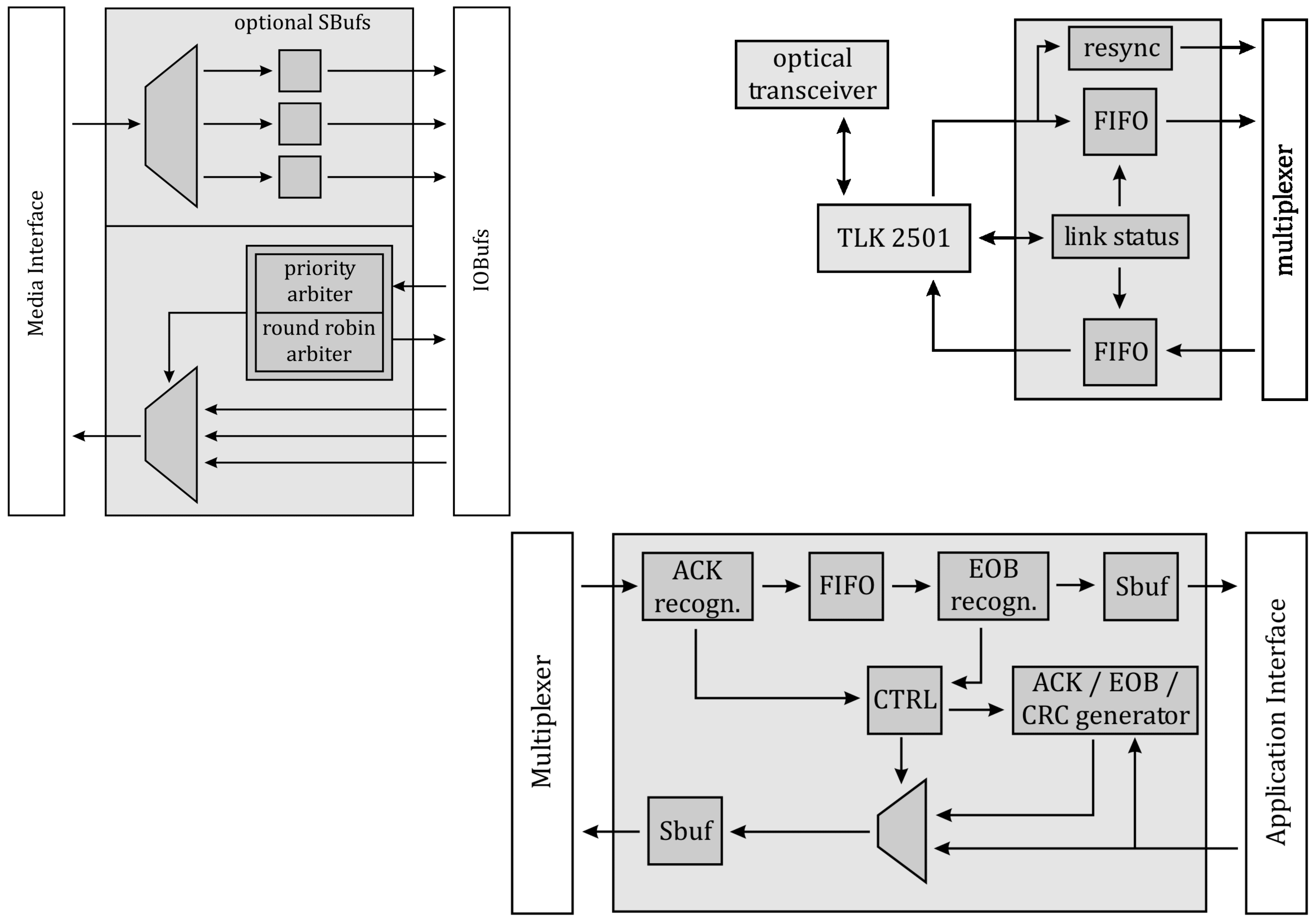

User
application
optional
IOBuf
IOBuf
IOBuf
hub logic
API
API
hub control


Init IBuf
Init OBuf
active port
control
packet
routing
arbiter
TRM concentrator
Reply OBuf
Reply IBuf
HDR resend

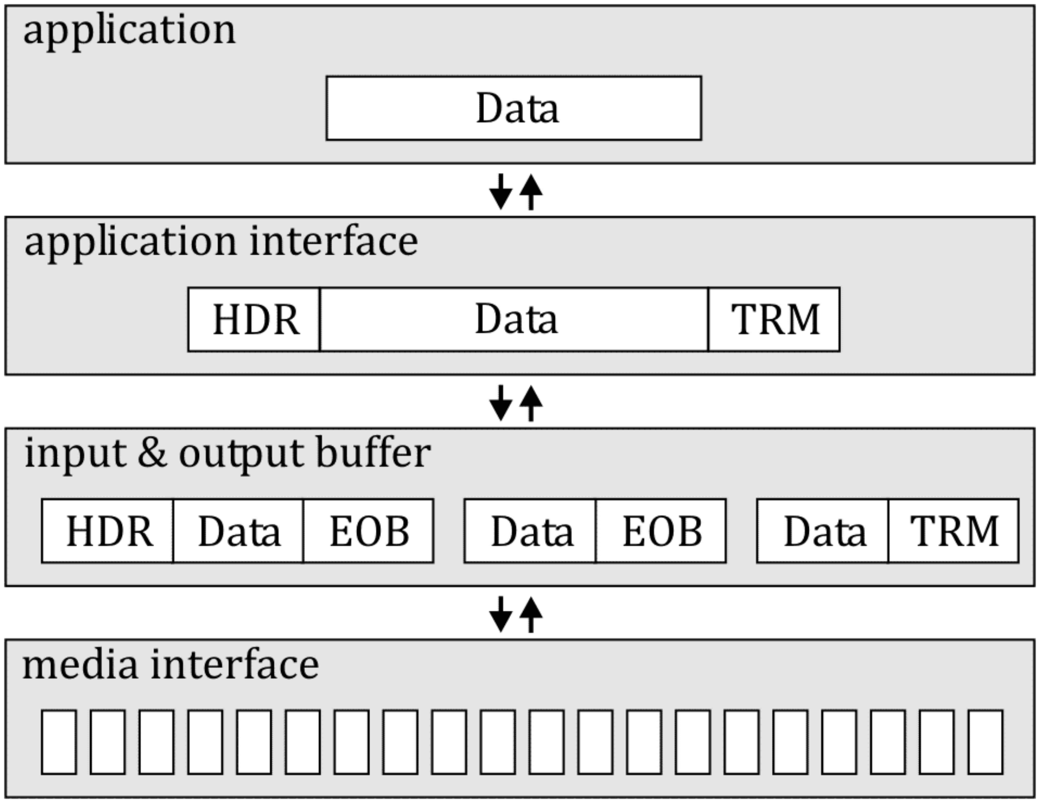
RegIO

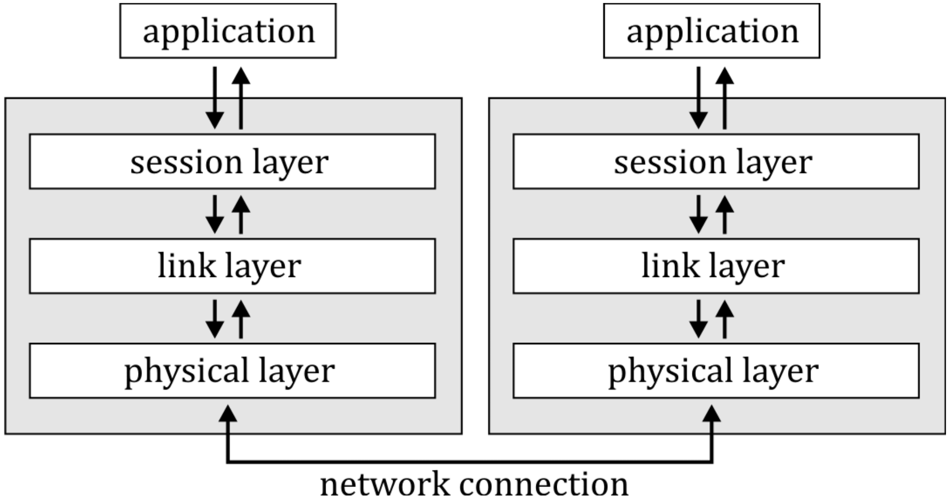

1-wire interface
Unique ID
ID RAM
Address
address controller
API
register controller
internal data port
board ROM
status register
control register
application

Multiplexer / IOBuf / MedTLK



Network Layers





Registers & Packet Types

Table B.1: Register Definitions

Name	Address		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Common Register 1	0000	l	error messages				trg mismatch		tbd									
		h	tbd				temperature											
Common Register 2	0001	l	trigger level 1 counter															
		h	trigger level 2 counter															
Board ROM 1	0040	l	compile time															
		h	compile time															
Board ROM 2	0041	l	compile version															
		h	compile version															
Board ROM 3	0042	l	Board information															
		h	Board information															

Table B.2: Packet type definitions

Name	Value	Description	F1	F2	F3
DAT	0	Normal data word	Data		
HDR	1	Header / Source change	Source Address	Target Address	sequence number / data type
EOB	2	End of Buffer	0	Data count	Checksum
TRM	3	Termination	Errorbits		sequence number / data type
EXT	4	Extended data word	checksum, other error detection		
ACK	5	Acknowledge		Length of Buffer	
—	6	—	—		
ILL	7	Illegal word	ignore		

Occupied Logic Resources

Table 6.4: Logic resources needed for a full featured network endpoint with four channels and slow control capabilities. The numbers given for the individual components do not add up to the given number of the whole endpoint due to optimization processes done by the synthesis tool and differences in the configuration used on different channels.

PART	NUMBER	SLICES	FF	LUT	BRAM
optical Media Interface	1	250	350	360	2
Multiplexer	1	170	90	320	0
IOBuf[a]	4	240	240	450	1
full API	3	280	300	510	2
trigger API	1	30	40	50	0
Slow Control	1	360	320	620	0
Full Endpoint	1	2050	2300	3600	10