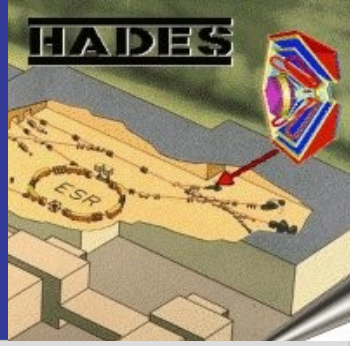

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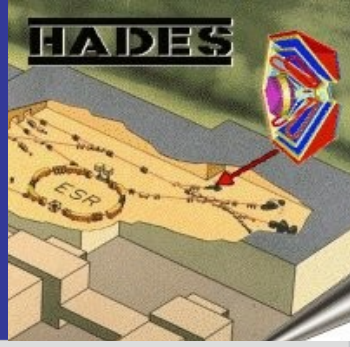
The General Purpose Trigger and Readout Board (TRB)

A step towards a FAIR DAQ

I. Fröhlich, M. Traxler, M. Kajetanowicz, K. Korcyl, W. Krzemien, M. Palka,
P. Salabura, C. Schrader, H. Ströbele, J. Stroth, P. Skott, A. Tarantola, R. Trebacz

Motivation I



- HADES is using a 2-level trigger system
- Level1: Multiplicity trigger
  - Trigger signal has to be fast
- Level2: Online search for lepton candidates
- Rates and downscaling for light systems (C+C):

	max. LVL1	*max. LVL2*	*LVL2 Trigger downscaling factor*
pulser rate	17kHz	4–5kHz	10–20
in beam	8kHz	1 kHz	10–20

- Goal: 20kHz in beam also for heavier systems (FAIR-HADES @ 8AGeV)
- HADES upgrade ongoing [1]
  - Includes detector upgrade (e.g. RPC, ForwardWall)

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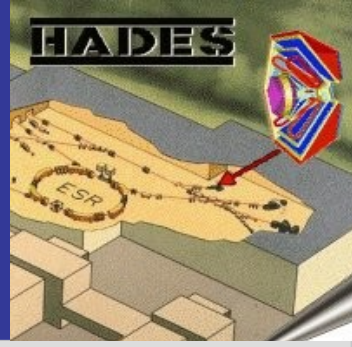
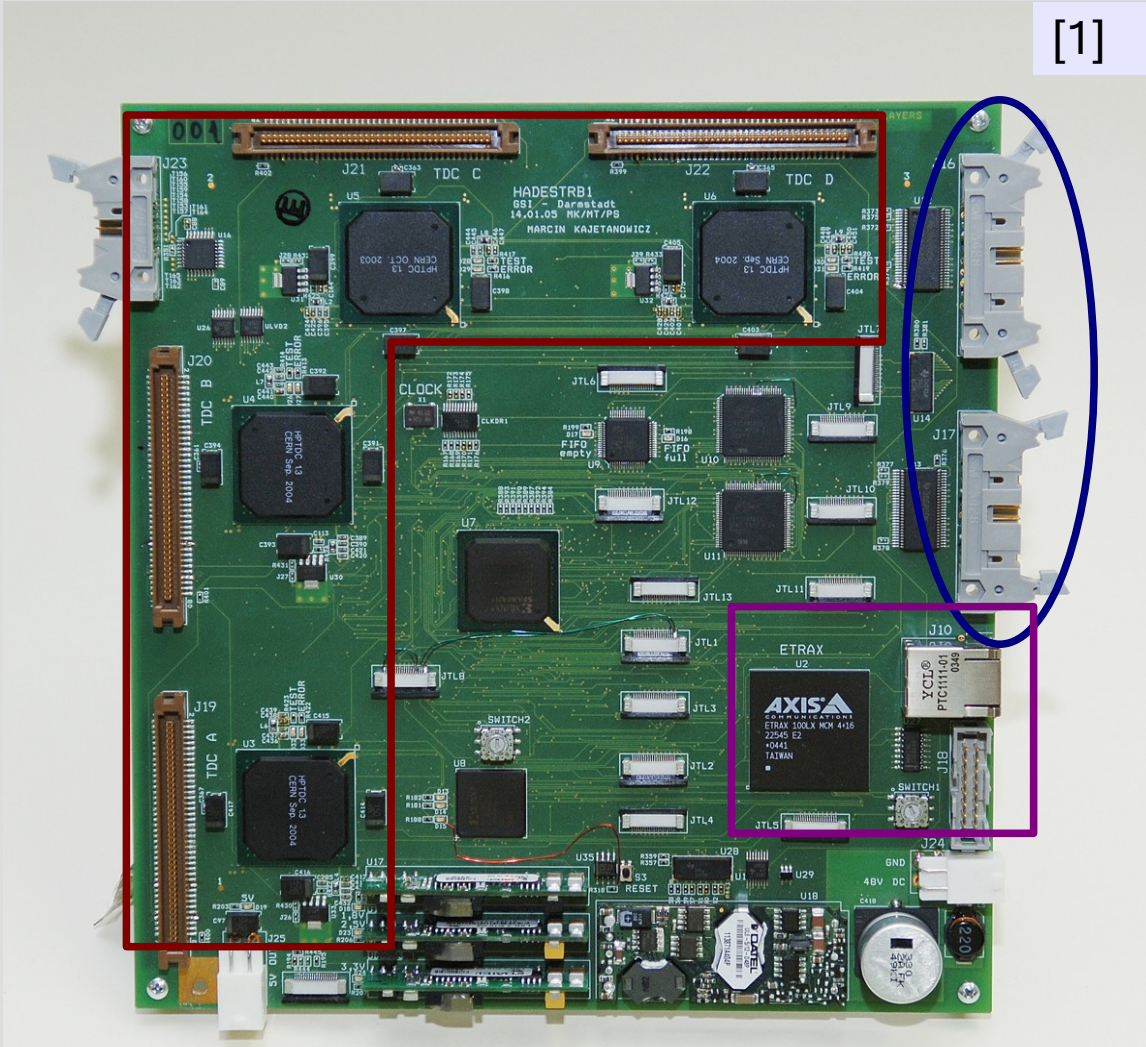
[1] supported by the EU under contract EU-CNI (construction) contract „DIRAC-PHASE-1“ 515876

TRB v1.0
Readout for RPC



- 128 channel TDC based on **HPTDC** [2]
- On-board DAQ functionality via **ETRAX** (Linux single chip computer) [3]
- 100MBit interface
- Access to **old** HADES LVL1 & LVL2 bus
- Succesfully integrated into HADES DAQ
- But only readout functionality

[1]



[1] M. Traxler , D. Gil, M. Kajetanowicz, K. Korcyl, M. Palka, P. Salabura, P. Skott, R. Trebacz: GSI Report 2006
[2] HPTDC, Jorgen Christiansen, Digital Microelectronics Group, CERN
[3] www.axis.com

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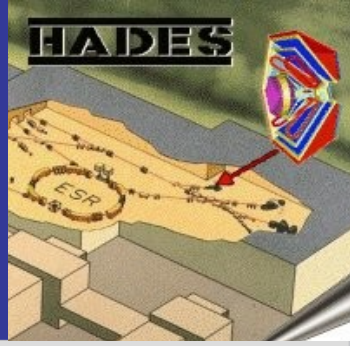
Motivation II



- TRBv1 shows that concept is working
- But needed:
  - Replacement of the old flat bus cable
    - no link control, no monitoring
  - Optical cable (2GBit) + LVDS connection + ...
  - DSP & bigger FPGA needed for online trigger algorithms
  - Individual add-on modules
    - e.g. MDC, RICH -> No TDCs
- Boundary conditions:
  - System has to run End 2008

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TRB and HADES

Central Trigger System (CTS)

Root VME-CPU
Central Monitoring
MU algorithm

Acromag

TRBNet

VULOM3

GP-AddOn

TRBv2

Trigger Sources

ATCA compute node

Optical Network

TRBNet

Readout-VME-CPU

TRB

TRBNet

Detector Trigger System (DTS)

Frontend Readout

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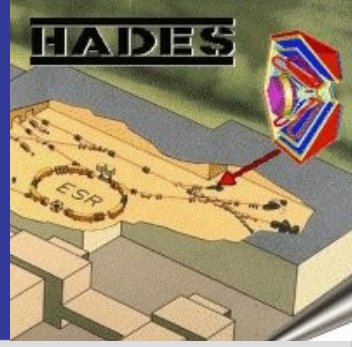
TRBv2



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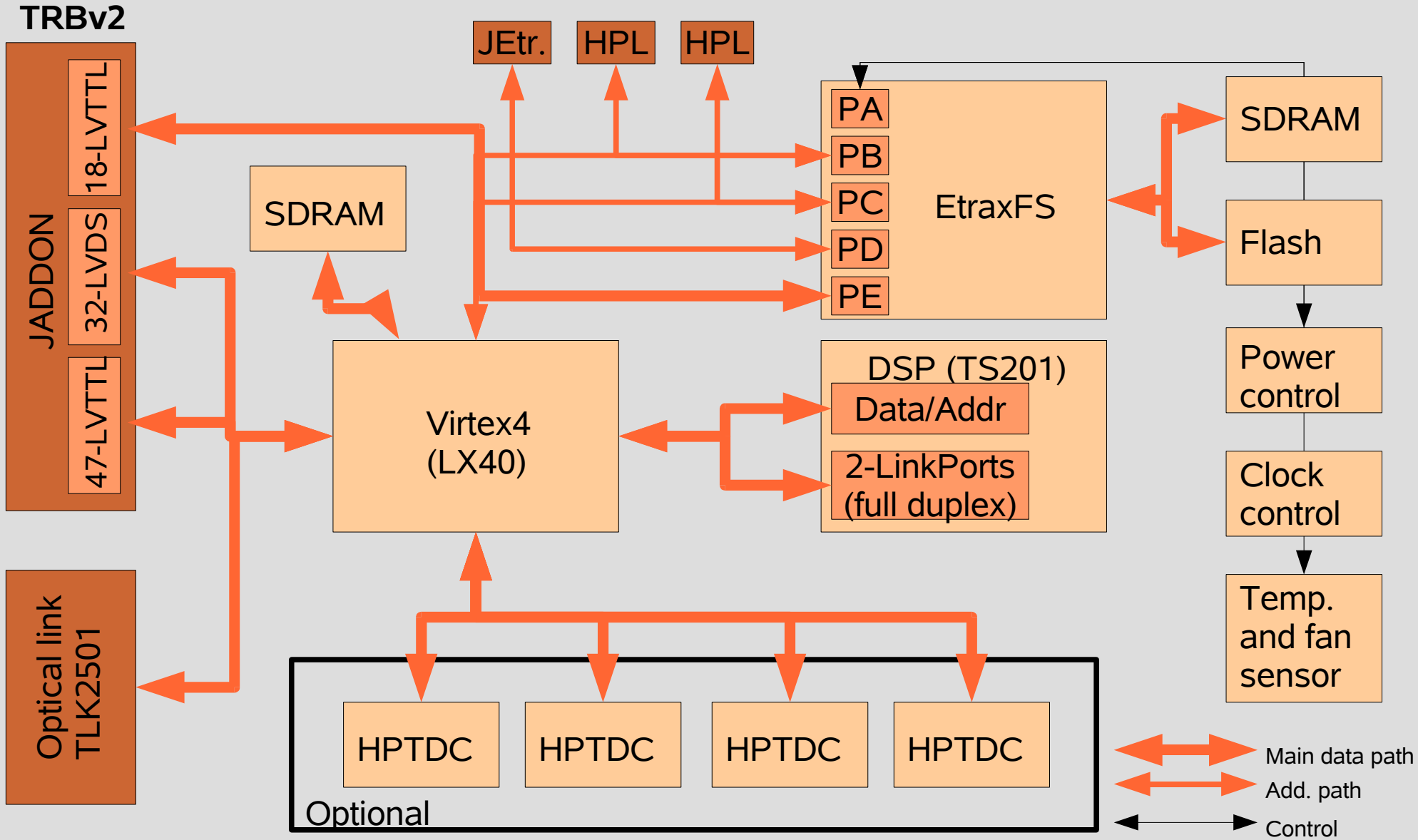
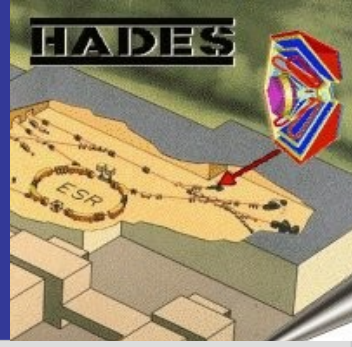
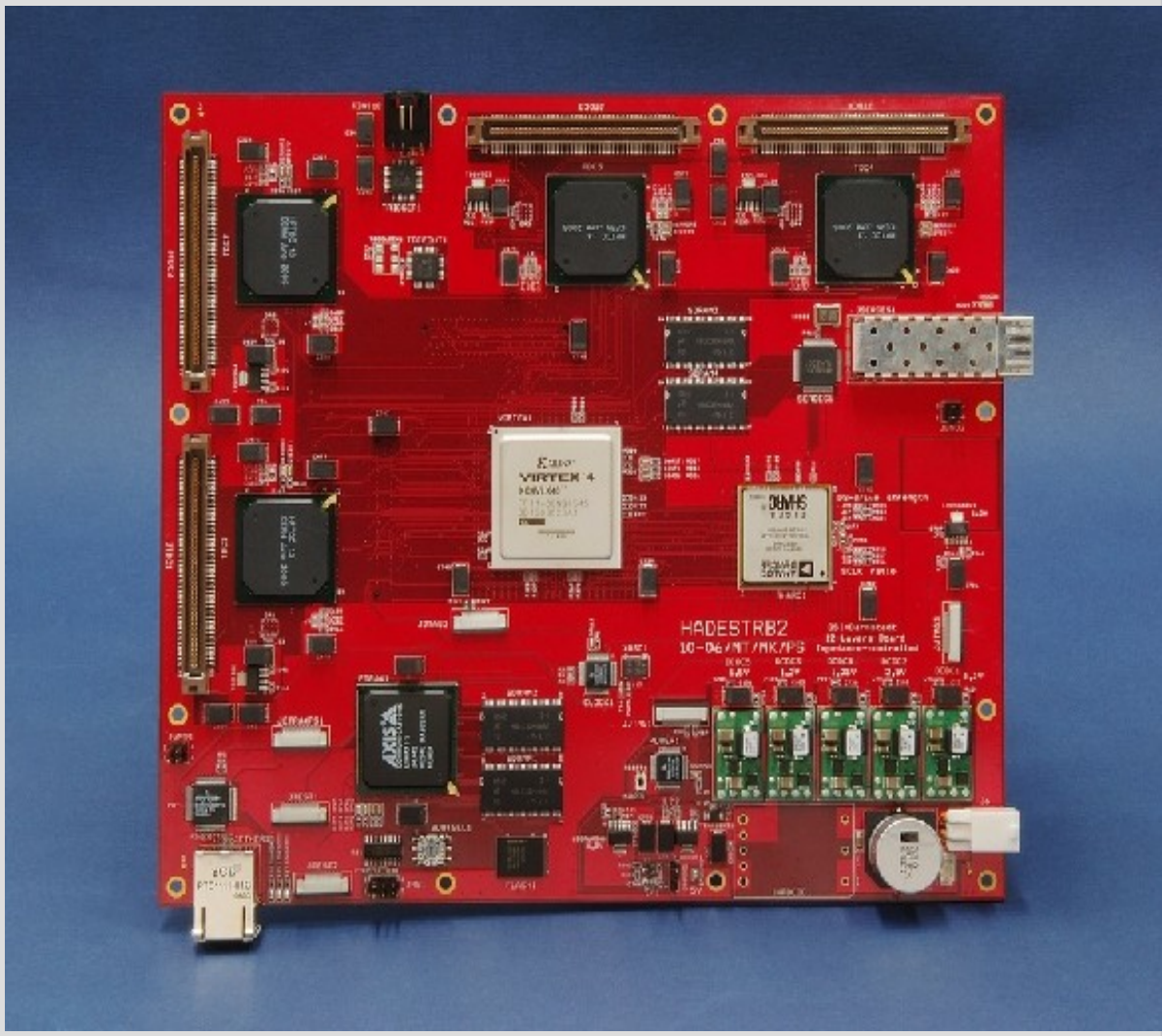


More Features



- TRBv2
- Engineering run „2a“
- Testing ongoing since Jan07
- AddOns (so far)
  - „general purpose“: IO signals
  - MDC-V1
- Updated version „2b“ ordered



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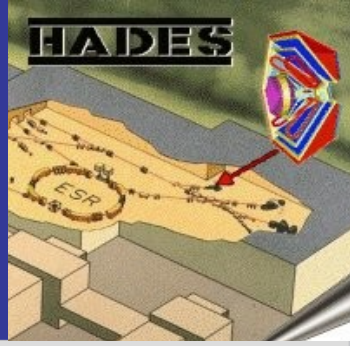
Our Ideas



- TRB-Collaboration
  - GSI-EE: Long-term support, infrastructure, knowledge base
  - Universities: Manpower (phd-students), sub-project leading (concept, ideas)
  - Integration of detectors (real environment)
- HADES-DAQ „next generation“
- Test for a distributed trigger system
  - Units -> System
  - IPUs -> „virtual“ Algorithms, shared ressources
  - Private communication -> homogenous network (TRBNet)

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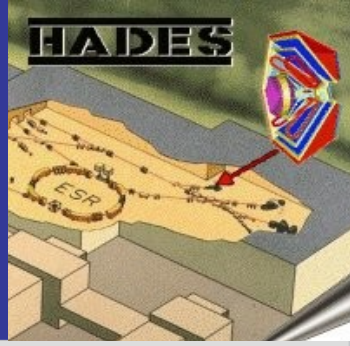
TRBNet Requirements



- Low latency (1-2µs in total)
- Trigger submission -> No data loss
- Any medium (Optical/polymer fibre, LVDS for VME-integration, AddOn
- Support for any FPGA (Virtex4, LatticeSC)
- Adaptable (e.g. buffer size vs. FPGA ressources)
- Busy-Logic included -> Several „channels“ are needed

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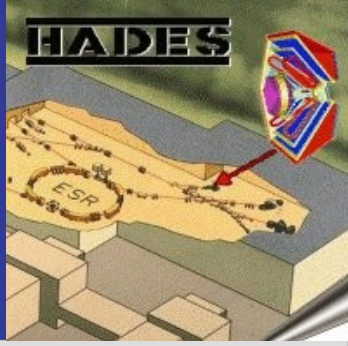
Goals and Milestones



- MDC-Addon
  - V1: Replacement of the readout chain
    - Currently implemented by A. Tarantola -> approx. 1y
  - V2: New communication cables
    - Polymer-optical-fibre? LVDS? -> will be started soon
- Shower-AddOn
  - M. Kajetanowicz
- RICH-AddOn
  - M. Böhmer (Munich) -> 2007 – mid2008
- Time-of-Flight (TOF): 2 possible roads
  - TRBv2 with TDCs
  - Using VME-based CPU + LVDS links
    - (Summer 2007)

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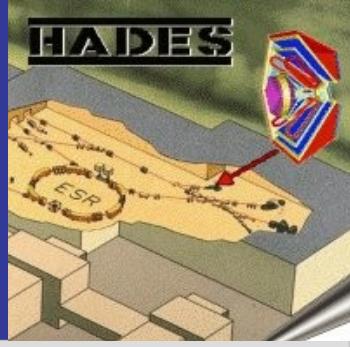
Connection to FAIR / Conclusion



- A complete new trigger system:
  - our „playground“
- TRBv2 will be used for PANDA-MDC
  - Testing of PANDA-compute node (W. Kühn)
    - Online tracking (HADES -> PANDA)
- Testing of Mimosa Readout
  - C. Schrader, since Jan07
- Testing of streaming (=triggerless readout)
  - Behaviour, bottlenecks etc...
- ...
- Reports (caveats, problems, conclusions, progress) are important for new projects