The new HADES Trigger and Readout System

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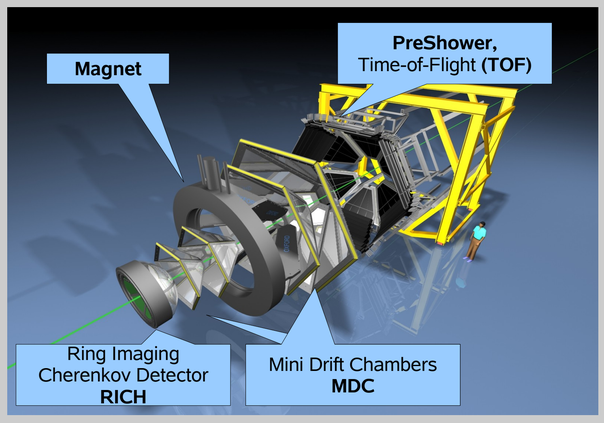
HADES

- Measurement of di-lepton pairs (e^+e^-)
- A+A, p+p, p+A, π+p, π+A



Motivation

- Heavy ion collisions (Au+Au) up to 8AGeV
- Integration of new detectors
  - Forward Wall (FW)
  - Resistive Plate Chamber (RPC)
- Upgrade of DAQ-System
  - Reduce LVL1 dead time
  - Improve LVL2 trigger data bandwidth
  - Trigger algorithm should be more selective
- Different hardware for each detector → not easy to maintain
- VME based readout → not scalable

TRB with TDC configuration

- 124-channel Time to Digital Converter (TDC) electronics
- Uses the HPTDC chip [1]
- Main usage: RPC-detector upgrade of the HADES-detector (2600 channels)
- Time resolution of <100ps required
- Measurement of Time-over-Threshold (TOT)
- First version TRBv1 successfully integrated into HADES-DAQ (Beamtime Apr06)

[1] HPTDC, J. Christiansen, Digital Microelec. Group, CERN

Add-On modules

- Possible options for connections to the front end electronics
  - Polymer optical fibre
  - LVDS

Full upgraded DAQ system

- 24 TRBv2 for RPC
- 24 TRBv2 for MDC
- 6 TRBv2 for TOF
- 6 or 12 RICH-TRBv2
- 6 TRBv2 for Shower-Readout
- 3 TRB for Forward-Wall
- 4 TRB for Pion-Hodoscopes

H-QM Helmholtz Research School Quark Matter Studies

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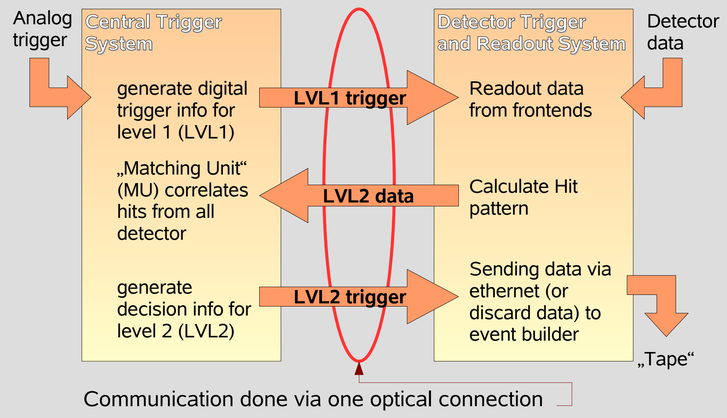
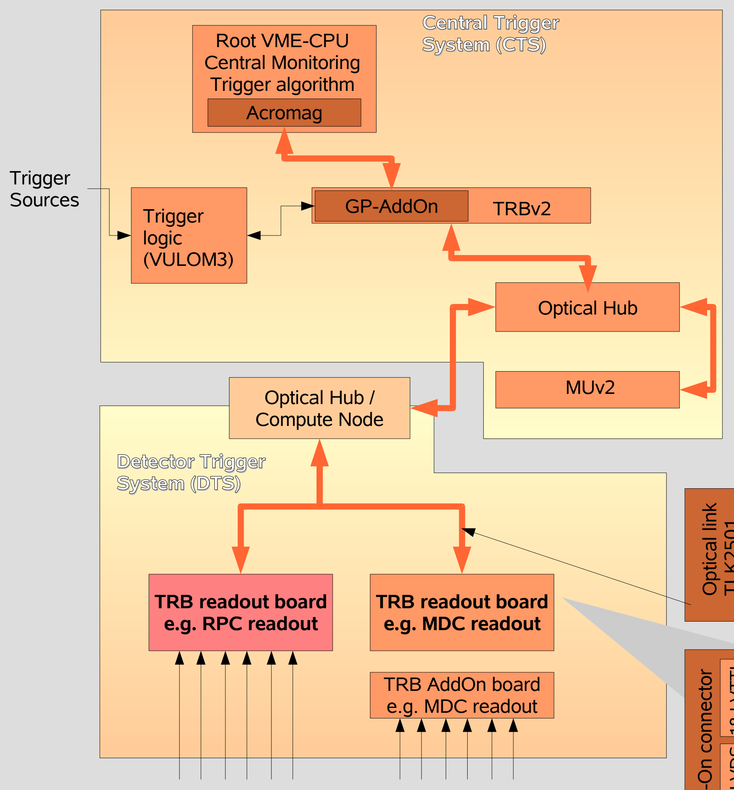
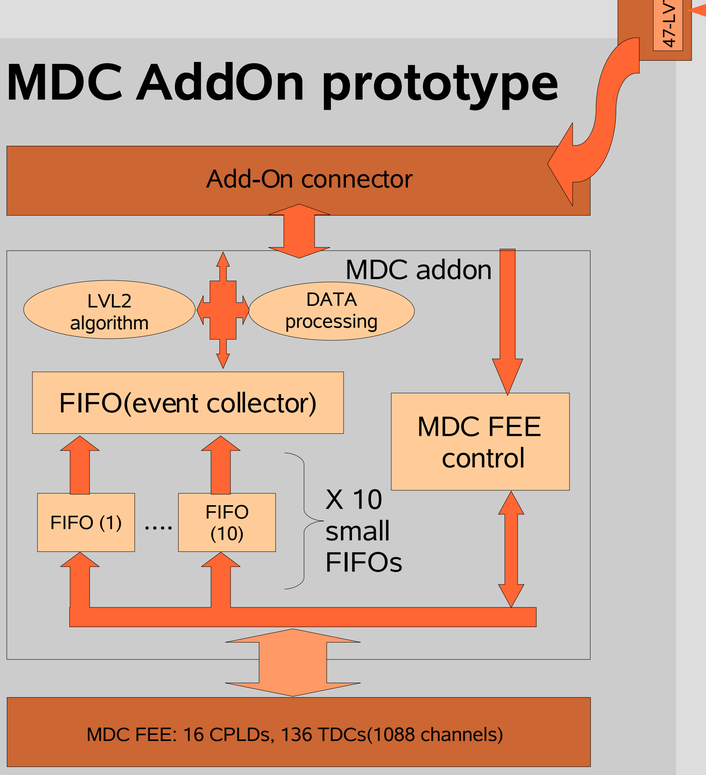
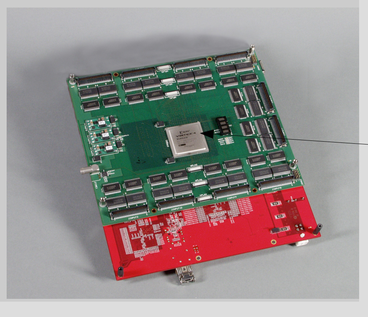




MDC AddOn prototype



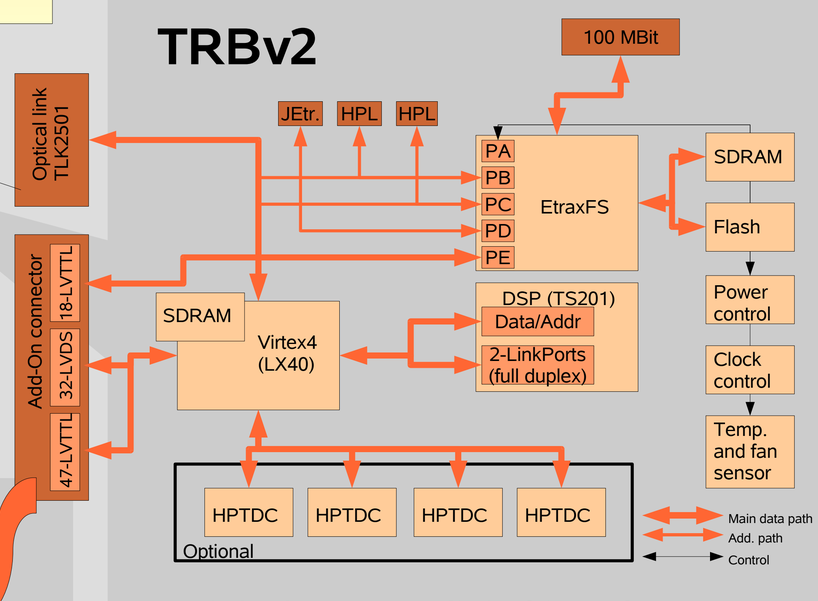
- Concept using AddOn modules: first version
- Equipped with 10 connectors, 50 pins each and 20 RS485 transceivers (SN75976A2DL).
- From each connector a standard RS485 bus is driven to the front end driver cards, which are placed on the HADES chamber main frame.
- A large FPGA (Xilinx Virtex4 XC4VLX-10FF1148) is placed in the center of the AddOn card.
- MDC AddOn (v2) final concept: studies ongoing



Concept

- Unified readout board for all detectors (**TRBv2, „Trigger and Readout Board“**)
- Detector dependent AddOn boards for the readout of the FEE, LVL1 and LVL2 pipes.
- Data transport is done by Ethernet.
- Readout hardware moves to the FEE. No long cables from the detector to the ADC/TDCs.
- Tree structure of the trigger system, only point to point links, realized with optical links and LVDS.
- Same link will be used for data transport for the LVL2 trigger (online hit pattern, tracks).
- Trigger-Hubs → trigger data processing

TRBv2

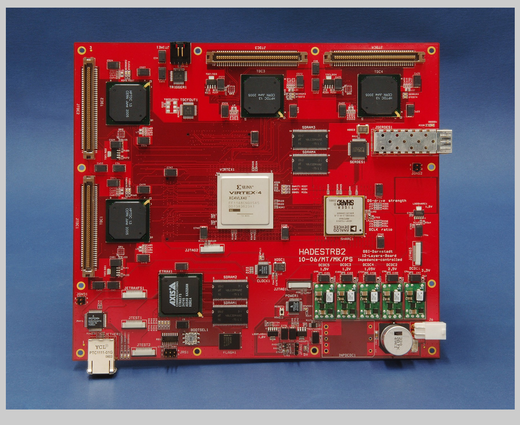


- High data-rate digital interface connector (15 Gbit/s)
- Possibility to mount AddOn boards for detector-specific interfaces
- Optical link (2 Gbit/s) based on TLK2501 from Texas Instruments
- FPGA (Xilinx Virtex4 LX40 + 128 MBytes RAM)
- TigerSharc DSP (Analog Devices) can be used as on-board resources for trigger and on-line analysis algorithms.
- Etrax-FS processor [2] for DAQ and slow-control functionality.
- Supports EPICS to allow the integration into the HADES Slow-Control System

[2] ETRAX, AXIS Communications, Sweden

Status

- Prototype TRBv2 produced and tested



- MDC AddOn v1 produced
- „general purpose“ (GP-AddOn) with various IO connectors (e.g. LVL1 trigger sources) produced and tested

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