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Field programmable gate array based data digitisation with commercial elements

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ABSTRACT: One of the most important aspects of particle identification experiments is the digitisation of time, amplitude and charge data from detectors. These conversions are mostly undertaken with Application Specific Integrated Circuits (ASICs). However, recent developments in Field Programmable Gate Array (FPGA) technology allow us to use commercial electronic components for the required Front-End Electronics (FEE) and to do the digitisation in the FPGA. It is possible to do Time-of-Flight (ToF), Time-over-Threshold (ToT), amplitude and charge measurements with converters implemented in FPGA. We call this principle come & kiss: use **CO**mplex Com**ME**rcial Elements & **K**eep **I**t **S**mall and **S**imple.

KEYWORDS: Front-end electronics for detector readout; Digital electronic circuits; Data acquisition circuits

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1 Introduction & motivation

Particle identification in nuclear physics experiments requires the digitisation of analogue data generated by the detectors, such as time, amplitude and charge information. Until now, the digitisation of data has been done mainly by Application Specific Integrated Circuits (ASICs), which require a long time and a lot of resources for development. However, with the recent developments in the Field Programmable Gate Array (FPGA) technology, it is now possible to use FPGAs for data digitisation.

The advantages of using FPGAs for such purposes are the availability of the products over the upcoming years, the high quality circuit design, the package and the easily accessible detailed documentation of the products. Because of the high portability of the digital designs, using an FPGA, also has the advantage of being vendor independent.

In order to use the FPGAs for data digitisation, we "misuse" the **CO**mplex and com**ME**rcial FPGAs, which are used mainly for digital circuit design, in the asynchronous and analogue domain. This way we use an FPGA as a Time to Digital Converter (TDC) to achieve time measurements with high precision. We also use the internal LVDS receivers of the FPGAs as discriminators eliminating any extra discriminator components, external components — Digital to Analogue Converters (DACs), Analogue to Digital Converters (ADCs) and Charge to Digital Converters (QDC) — for the necessary Front-End Electronics (FEE) depending on the kind of the measurement we would like to make and we keep the number of them to the minimum. We **K**eep **I**t (the design) **S**mall and **S**imple: we name this concept *"COME & KISS"*.

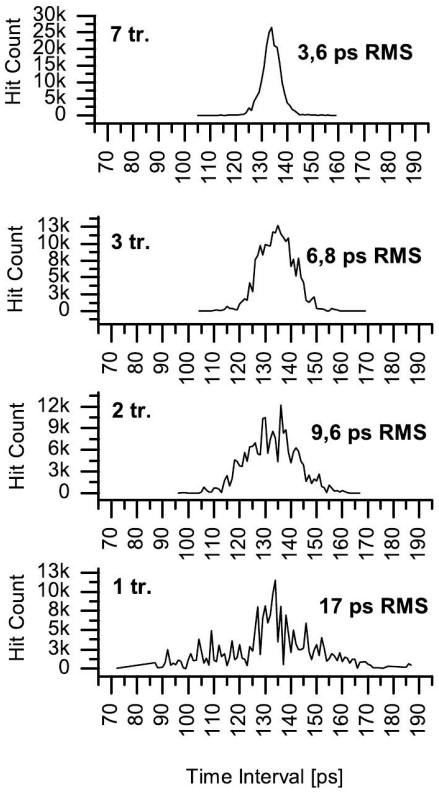

Figure 1. Effects of number of transitions on the TDC precision. [3]

2 Time digitisation in FPGAs

In order to measure the time intervals with high precision we used the Tapped Delay Line method, which uses the basic building blocks of an FPGA. This method is chosen, as it best suits the architecture of an FPGA. The details of the implementation can be found in [1]. Using this implementation we achieved 17 ps (RMS) time precision between two channels of the TDC.

It is shown in [2], that by using a method called Wave Union it is possible to increase the resolution of the TDC beyond its intrinsic cell capabilities, thus yielding an improvement in the precision. This method is based on increasing the number of measurements — transitions — within the FPGA for a single time measurement. By increasing the number of transitions and adjusting the time difference between the transitions it is possible to achieve significant improvements in the resolution and the precision.

A study [3] is carried out based on this principle and the effect of increasing the number of transitions is shown. As it can be seen in the figure 1, it is possible to increase the precision up to 3.6 ps by using 7 transitions.

Of course this performance comes with a trade off of the number of channels ($\sim$5 times less channels) and dead time ($\sim$20 times longer dead time). In our implementation we kept the number of transitions at 2 achieving a time precision of $\sim$10 ps (for single clock cycle time intervals) and number of channels of 65 (figure 2b). We realised this design on the TRB3 (TDC Readout Board). The board has 5 Lattice ECP3-150EA FPGAs, four of them are used for TDC realisation reaching

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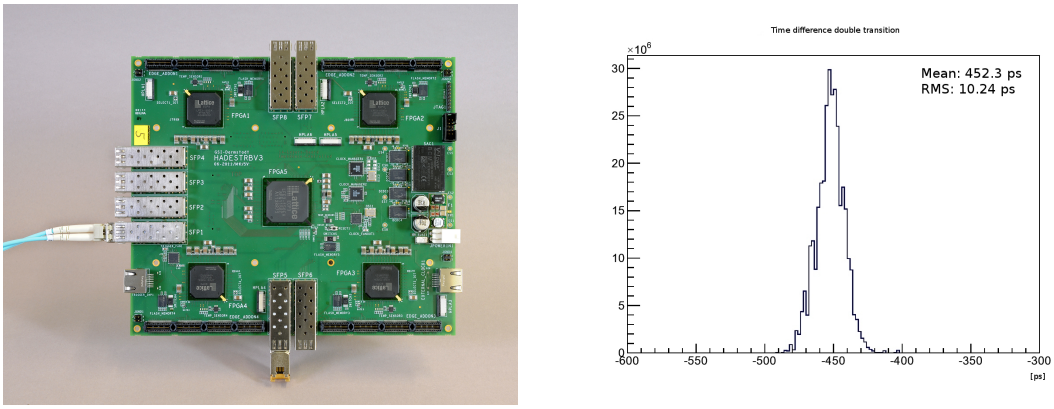

(a) (b)

Figure 2. 2a TRB3 with 260 channels in 4 FPGAs. 2b TDC precision with 2 transitions.

a number of 260 channels (figure 2a). The central FPGA is used for our special network called TrbNetwork [4] for data acquisition, slow control and trigger. Direct GbE connection is also done via this FPGA. The board can cope with a hit rate of 50 MHz (in a burst) and a data readout trigger rate of 300 KHz. The board is designed to be used in large systems using the TrbNetwork as well as a stand alone system with only a 48 V power supply and the GbE implementation in the central FPGA in order to send data out to a PC. Thanks to the flexibility of the FPGAs, the peripheral FPGAs can also be used as concentrators with suitable passive AddOn boards connecting many boards together. The TRB3 is suitable for Time-of-Flight (ToF) and Time-over-Threshold (ToT) measurements, where the time information is encoded in the discriminated detector signals.

3 Signal discrimination using FPGAs

Modern FPGAs provide better internal components, such as LVDS receivers and drivers, with high quality and performance. With this advantage in hand one can use the internal FPGA components out of their normal function. It was therefore decided to use the LVDS receivers of the FPGAs as discriminators, thus eliminating any excess external discriminators and minimising the design.

3.1 Signal discriminator board

The FEE board we developed (figure 3) uses commercial amplifiers (Monolithic Microwave Integrated Circuits — MMICs) at the amplification stage of the signals from the detector with an amplification factor of 40. The amplified signals are discriminated against the reference voltage at the LVDS input buffers. The time information of the leading edges and the time-over-threshold of the detector signals are encoded in the digital pulses in the FPGA. These digital pulses are sent out as differential signals via the LVDS output buffers for time measurements. In order to set the thresholds at the LVDS receivers the FPGA is used as a DAC via a Pulse Width Modulator (PWM) and low pass filter. The discrimination board is connected directly to the detector outputs.

During our tests we applied a 6 ns wide 500 μV analogue signal to the board as an input signal. We set the threshold level to the right level with a resolution of $< 100\,\mu$V. After the amplification

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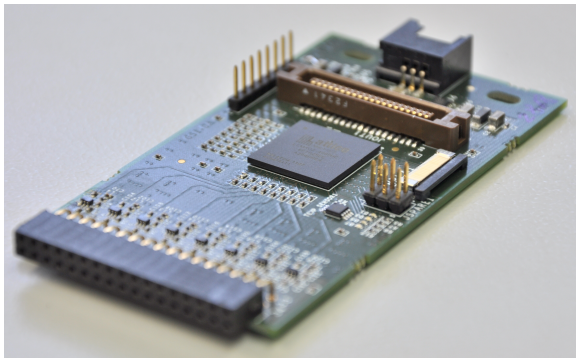
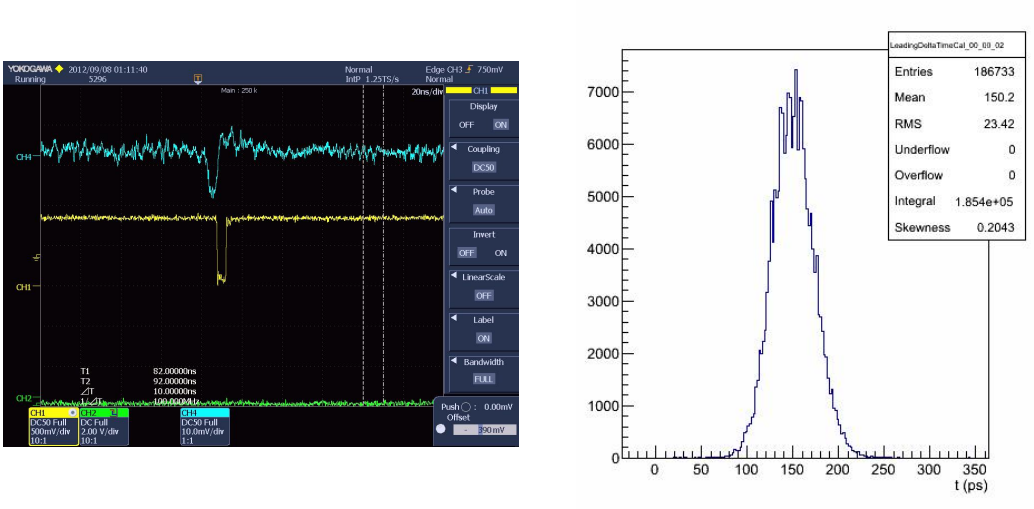


Figure 3. Signal discriminator board using a commercial FPGA.



(a) (b)

Figure 4. 4a The analogue signal is discriminated at the LVDS receivers of the FPGA and sent out for time measurements as a digital LVDS signal. 4b The precision of the whole system — discriminator board and TRB3 — is measured as ∼23 ps.

and discrimination we sent the digital LVDS pulse (figure 4a) to the TRB3 with TDC designs for time measurements and we reached a time precision of ∼23 ps RMS (figure 4b).

Keeping our design small and simple and using commercial components, we developed our 16 channel discriminator board with a cost of €0,56 per channel (component costs). The performance of the board will be verified with the real signals from the 2400 channel Photo-multiplier Tube (PMT) and Multi-Chamber Plate Photo-Multiplier Tube (MCP-PMT) detectors during the upcoming experiments with beam.

3.2 Signal discrimination and time measurement on the same board

In order to minimise the whole system and make it more compact we also developed a board, where the FEE — amplification and discrimination — is integrated with the time measurement, data acquisition and power (figure 5).

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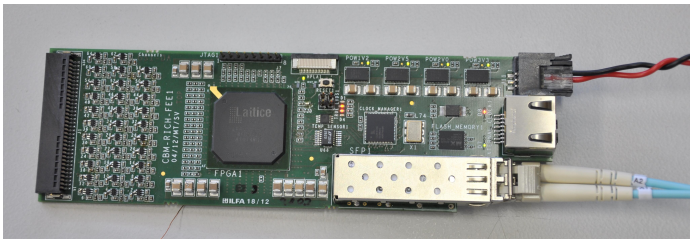
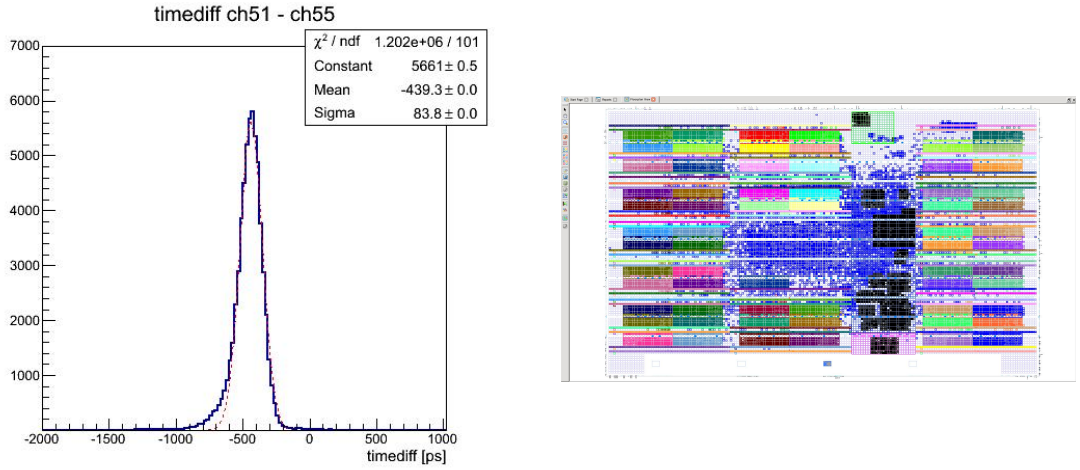


Figure 5. Signal discriminator board using a commercial FPGA.



(a) (b)

Figure 6. 6a Precision measurement result of the FEE board – ∼84 ps. 6b The layout of the 65 channel TDC in the FPGA.

On this board the amplification of 64 signals from the detector occurs right after the input connector. Again, these signals are discriminated at the LVDS receivers. The threshold levels are set by using a commercial DAC (Linear Technology – LTC2620) on the board via slow control channel of the TrbNetwork. The time information from the discriminated digital pulses is measured with a 64 channel TDC implemented in the same FPGA (figure 6b). The time information of the trigger signal is also measured at the 65th channel of the TDC. The measurement results are readout via a 2 GBit/s optical link. This highly compact board (5 cm × 16 cm) is designed to be plugged directly on the MCP-PMT.

The precision of the board is measured with an analogue signal from a pulse generator connected at the input connector as the analogue signal. Due to the layout errors at the amplification stage, small oscillations occur at the outputs of the amplifiers and reduce the time precision to ∼84 ps RMS (figure 6a). The performance of this board also will be measured during the upcoming beam times.

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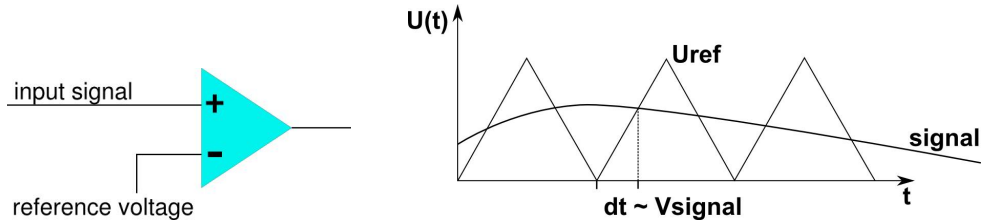
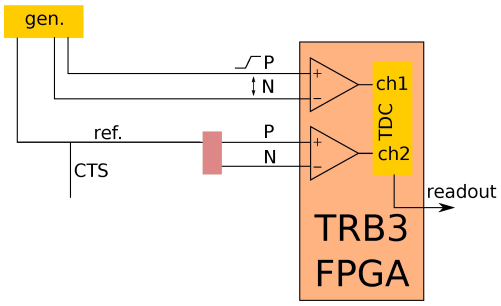


(a) (b)

Figure 7. The input signal is compared to the reference ramp signal and the reference crossing times are encoded in the digital pulse.



Reference Vol. (mV)	Mean (ps)	Jitter (ps)
400	2551	50
800	3034	24
1200	3538	18
1600	4125	15

(a) (b)

Figure 8. ADC measurement diagram and results.

4 Amplitude digitisation in FPGAs

For amplitude digitisation using an FPGA one can use the LVDS receivers as discriminator but this time against a linear ramp signal with a known frequency (figure 7). The LVDS input buffer will create a digital pulse at its output, where the reference voltage crossing times are encoded in the edges of the pulse. By measuring the time difference of the edges of this digital pulse compared to the start of the ramp signal it is possible to calculate the voltage at the input pin. For the time measurements the designed TDC can be used in the same FPGA.

For a 10-bit ADC with 50 MS/s sampling rate a time precision of 20 ps is necessary. The advantages of such a design are to have many channels in one FPGA, no extra data transfer to the FPGA for the time measurements, thus consuming lower power.

For ADC switching characteristics test purposes we generated the ramp signal externally and applied it to one channel of the TDC in the FPGA. We altered the reference voltage at this channel and used the reference signal from the pulse generator as trigger (figure 8a). We measured the time difference between the two channels and recorded the time precision (figure 8b).

The conclusions from our first measurements are, that the ADC in FPGA concept works and the measured TDC time precision with the 26 ns ramp signal is sufficient for a 10-bit ADC with 20MS/s sampling rate. But there is a dependency on the time precision of the TDC and the ADC input voltage level. For further quality tests of this ADC in FPGA concept, a ramp generator on the board has to be implemented.

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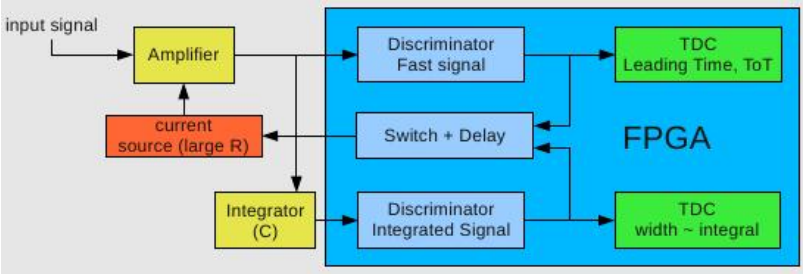

Figure 9. The concept of the QDC is based on a modified Wilkinson ADC.

5 Charge digitisation in FPGAs

Our idea of QDC is based on a modified Wilkinson ADC: the analogue input signal from the detector is integrated using a capacitor and it is discharged linearly using a current source, thus achieving a fast crossing of the threshold and therefore a better charge precision compared to a RC-discharge (figure 9). The width of the digital pulse is measured using an FPGA-TDC, delivering the time measurement of the leading edge as well as the charge encoded in the length of the pulse.

Based on this concept a prototype board is developed with 4 channels. The first results show that 0.2% charge precision is possible with an offline calibration. The dynamic range of the prototype is 50. The oscilloscope screen-shots of two analogue signals with 1 mA and 2 mA peaks and corresponding integrated and discriminated signals are shown in figure 10b and 10d. The width of the digital pulse for the 1 mA input signal is measured as $\sim$68 ns, whereas the pulse width of the signal for the 2 mA input signal is $\sim$100 ns.

6 Conclusion & outlook

A multi-purpose FPGA based TDC module (TRB3) with 256 TDC channels and 4 reference time channels reaching a time precision of $\sim$10 ps RMS (in one clock cycle interval) has been developed and commissioned successfully. A trigger system for external and internal triggers and a GbE module for direct data acquisition to a PC have been integrated in the central FPGA of the board. With these modules a power supply and an Ethernet cable for the data acquisition is sufficient for a stand-alone system. Thanks to the re-programmable flexible FPGAs, it is also possible to combine many boards in a system to build large setups.

FPGA based signal discriminator boards have been developed and tested successfully. A highly integrated board with FPGA based discriminators and TDCs has also been developed. The advantages of these boards are that they can be plugged directly on the detectors as well as they are very compact, simple, flexible and easily available (only commercial components). Delivering full digital signals from these boards is another advantage. On the other hand, the performance of the LVDS receivers as discriminators is not as good as dedicated discriminators. Also this solution is larger that a tailored ASIC solution.

As further development leading and trailing edge detection of a digital pulse in a single TDC channel is under development. This development will double the number of channels for ToT measurements. FPGA based ADC design using FPGA based TDCs is also under development. The

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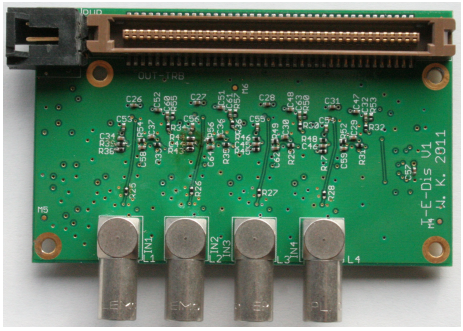
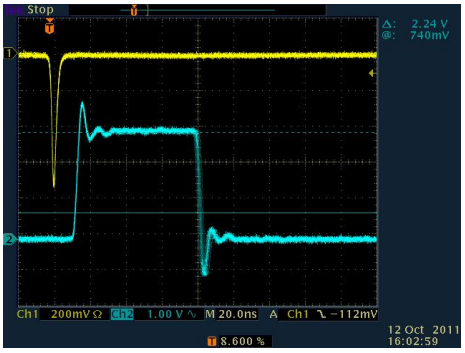
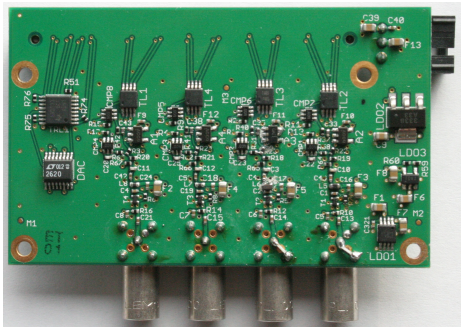


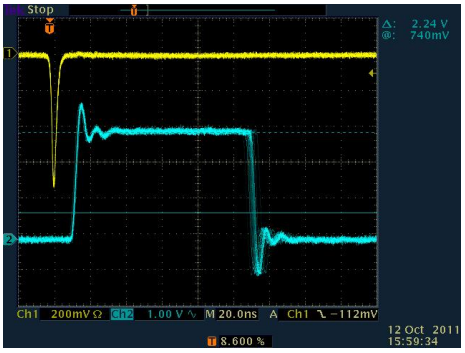
(a) QDC prototype board — Front view.



(b) The pulse width of the integrated signal of a 1 mA peak signal is measured as ∼68 ns.



(c) QDC prototype board — Back view.



(d) The pulse width of the integrated signal of a 2 mA peak signal is measured as ∼100 ns.

Figure 10. The QDC prototype board and output digital pulses integrated from the input signals.

TDC-based QDC prototype has been successfully tested and a system for a calorimeter application is in the design phase. The real world performance of the developments with many channels will be determined during the upcoming experiments with beam.

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