New Trigger unit based on the universal logic module (Jan Hofmann, GSI)

Draft specification V0.1, Nov 30, 2006, more details on request.

Revision history:

V0.1: Timing requirements for input/output signals added. Remark on scalers. Draft of an extension (12 additional inputs, 8 additional outputs) added.

In the first step the new trigger module should implement the following features:

External Inputs:

- 5 physics triggers (random input, rate < 1 Mhz)
- 1 timing signal TS (to gate the 5 physics triggers). Random input, < 10 MHz
- 1 veto signal VS (to veto the timing signal before further processing). Correlated with timing signal.
- Busy signal provided by the central trigger unit. Used to gate global trigger. Lemo input.
- Spill Start signal SST (for reset of internal scalers). Not used in the fast trigger part. Lemo Input.

Internal input:

- Clock signal

Delay and width of all external inputs need to be adjusted via remote control. All Inputs must have remote controlled downscaling (2**0 down to 2**14, turn off completely in the common Or output)

The timing signal TS (delay adjustable) must be vetoed by the Veto signal VS (after delay and width adjustment). The resulting gated timing signal (GTS) is used to gate all physics triggers.

The 5 physics triggers together with the timing and veto inputs and the internal clock input form a group of 8 triggers (TR0-TR7) which need individual downscaling before an OR of all 8 is performed to generated the global trigger (GT). TR7 is the downscaled clock trigger.

Outputs:

- Or of all Inputs (after individual downscaling and gating with GTS): GT.
- TR0 – TR6 before downscaling and TR0-TR7 after downscaling and busy gated. This allows to generate two groups of 8 outputs where the global trigger GT replaces the clock trigger before downscaling (no need for that).
- Two Multiplexer Outputs allowing to look at all input signals before and after (delay,width) adjustment, busy input, global trigger .... These signals should go to the two Lemo outputs.

Two times 8 scalers to monitor rates per spill (32 bits for the 8 triggers before downscaling, at least 16 bits for the 8 triggers after downscaling). Scaler contents are stored in registers after each spill signal SST. Registers are accessed via VME. Scalers are reset after the result is stored. Please note that the programmable downscaling of the Trigger outputs can be the first part of the 32 bit scaler.

Details:

All external inputs should be synchronized with a fast common clock (>= 300 Mhz). First shaped to a signal with width = 1 clock cycle, then delayed (shift register, programmable multiplexer), then adjusted in width (shift register with multiplexer connected to asynchronous FF reset). In order to make efficient use of the fast routing resources, it is perfectly fine if ALL remote controlled adjustments take place in an asynchronous way (driven by a slow clock not synchronized with the fast trigger timing part). This results in one or a few events being in undefined (screwed up) state after a readjustment via slow control. This is perfectly acceptable. My (limited) experience shows

that the time critical trigger part can be optimized much better (higher clock frequencies), if the slow control part is completely asynchronous and decoupled.

Timing requirements:

Input signals:

- All 5 physics triggers should allow for a programmable delay in between 0 ns and about 50 ns. Using a clock with frequency of 300 Mhz or 350 Mhz (aim at the latter), this corresponds to a 16 bit shift register.
- All 5 physics triggers should allow for a programmable width in between about 10 ns and about 50 ns. Using a clock with frequency of 300 Mhz or 350 Mhz (aim at the latter), this corresponds to a 16 bit shift register with only the last 13 bits accessible via a multiplexer.
- Timing signal TS: Width = 1 clock cycle. Programmable delay in between 0 ns and about 50 ns (see above)
- Veto signal VS: Width about 1 - 4 clock cycles (programmable). Programmable delay in between 0 ns and about 50 ns (see above)

Output signals:

- Global Trigger: No delay. Fixed width of about 40-50 ns.
- TR0 – TR6 before downscaling and TR0-TR7 after downscaling and busy gated: Fixed delay of about 80 - 100 ns. Fixed width of about 40 - 50 ns.

The delay refers to the global Trigger GT.

Extension:

In a second step, 2 * 6 inputs can be added. They contain sectorwise trigger inputs from an inner MDC plane and sectorwise inputs from TOF/Tofino/RPC, respectively. They are connected to two further input connectors.

These signals are shaped like the 5 physics triggers (delay, width) and a sectorwise AND is performed afterwards. The result is combined via a 6 fold OR and used to gate the global trigger GT. It should be possible to disable this gate via remote control.

In addition, these 12 signals can be used to address the fast SRam together with 4 of the 5 physics triggers. The SRam has 16 address bits and 16 output bits. 8 of the data output bits can be used to generate 8 additional output triggers by using the SRam as a lookup table. The output triggers are forwarded to an additional output connector.

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