Table 1-3. VMEbus pin assignments.

P1/J1			
Pin Number	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(††) SERCLK	A17
22	IACKOUT*	(††) SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 VDC	+5VSTDBY	+12 VDC
32	+5 VDC	+ 5VDC	+5 VDC

1.2.7.2 ACFAIL*

The AC power fail signal ACFAIL* is driven by the power monitor (functional module). When asserted, it signals to all modules that the system power source is about to stop. The use of ACFAIL* is optional. ACFAIL* is an open-collector class signal.

Table 1-3 (con't).

P2/J2			
Pin Number	Row A	Row B	Row C
1	User Defined	+5 VDC	User Defined
2	User Defined	GND	User Defined
3	User Defined	(†) RESERVED	User Defined
4	User Defined	A24	User Defined
5	User Defined	A25	User Defined
6	User Defined	A26	User Defined
7	User Defined	A27	User Defined
8	User Defined	A28	User Defined
9	User Defined	A29	User Defined
10	User Defined	A30	User Defined
11	User Defined	A31	User Defined
12	User Defined	GND	User Defined
13	User Defined	+5 VDC	User Defined
14	User Defined	D16	User Defined
15	User Defined	D17	User Defined
16	User Defined	D18	User Defined
17	User Defined	D19	User Defined
18	User Defined	D20	User Defined
19	User Defined	D21	User Defined
20	User Defined	D22	User Defined
21	User Defined	D23	User Defined
22	User Defined	GND	User Defined
23	User Defined	D24	User Defined
24	User Defined	D25	User Defined
25	User Defined	D26	User Defined
26	User Defined	D27	User Defined
27	User Defined	D28	User Defined
28	User Defined	D29	User Defined
29	User Defined	D30	User Defined
30	User Defined	D31	User Defined
31	User Defined	GND	User Defined
32	User Defined	+5 VDC	User Defined

Notes: (†) RESERVED was redefined as RETRY*, and (††) SERCLK & SERDAT* were changed to user defined pins in the proposed VME64 enhancements.

1.2.7.3 AM0-AM5

The address modifier code AM0-AM5 is driven by masters and interrupt handlers. It accompanies an address and indicates both the size and type of address transfer. It is used by slaves to determine which address lines should be decoded. AM0-AM5 are standard three-state class signals.

1.2.3.4 Utility Bus

The *utility bus* is a collection of signals used for system reset, periodic timing, system diagnostics and power failures. Signals of the utility bus include SYSCLK*, SYSRESET*, SYSFAIL and ACFAIL*.

1.2.3.5 Serial Bus

The VMSbus *serial bus* is used to pass urgent messages between VMEbus modules or systems. Two signal pins, called SERCLK and SERDAT* are used as clock and data lines respectively. The proposed VME64 bus specification reclassifies these pins as user defined. VMSbus can, however, still be implemented on these pins.

1.2.4 Data Transfer Cycles

VMEbus offers four types of data transfer bus cycles. This variety of cycles allow the bus to adapt to the changing requirements of the system.

1.2.4.1 Read/write Cycle

Read/write cycles are used to transfer 8, 16, 24 or 32-bits of data between bus modules. The cycle begins when the master broadcasts an address and an address modifier. When selected, slaves capture the address and respond to the cycle.

1.2.4.2 Read-modify-write Cycle

The read-modify-write cycle permits indivisible bus cycles. This cycle is especially useful for arbitrating shared resources in multiprocessor or multiuser systems with semaphores.

1.2.4.3 Block Transfer Cycle

The block transfer cycle moves a block of data between masters and slaves. Read or write block transfer cycles up to 256 bytes in length are permissible. This cycle is faster than READ/WRITE cycles because slaves are addressed only once (at the beginning of the cycle). It is especially useful for quickly moving large blocks of data.

The proposed VME64 specification now allows 64-bit (address and data) block transfer cycles of up to 2K-bytes in length.

1.2.4.4 Address-only Cycle

During the address-only cycle a master generates a valid address, but slaves do not respond (the master never asserts either data strobe). It allows slaves to decode an address at the same time that a master's on-board memory does, and speeds up the system.

1.2.5 Interrupt Acknowledge Cycle

The interrupt acknowledge cycle is initiated by interrupt handlers in response to interrupt requests. This cycle performs two functions: it passes STATUS/ID bytes and arbitrates the interrupt sources.

1.2.6 Arbitration Cycle

An arbitration cycle is performed during bus arbitration. It begins when a requester generates a bus request to the central arbiter. The arbiter grants the bus to the requester when the bus is not busy, and the requester acquires the bus by asserting the bus busy signal (BBSY*). The requester releases the bus by negating BBSY*.

1.2.7 Signal Summary

Table 1-3 shows pin assignments for the P1/J1 and P2/J2 backplanes. The P1/J1 backplane carries 24 address lines, 16 data lines, all control signals and some of the power and ground traces. The P2/J2 connector carries the extra eight address and 16 data lines, with additional power and ground pins. All of the defined P2/J2 signals are located on the center row of pins. The outer two rows of that connector are user defined, and can be used for any purpose. In general these are used for I/O signals or for a side bus such as VMXbus, VSBbus or VXIbus.

VMEbus uses an asterisk (*) following a signal name to show that its active (valid) state is logic zero. The absence of an asterisk means that its active state is logic one. When a signal is edge sensitive the asterisk shows that it is valid during the high to low transition of the signal.

Each VMEbus signal falls into one of five classes of electrical specification. These classes are called standard three-state, high current three-state, standard totem-pole, high current totem-pole and open collector signals. Chapter 6 describes the characteristics of these classes in detail.

1.2.7.1 A01-A31

The address bus (A01-A31) is driven by masters and interrupt handlers. During data transfer cycles they are used to broadcast short I/O (16-bit), standard (24-bit) and extended (32-bit) addresses. The width of the address bus is selected by masters with the address modifier code AM0-AM5.

The proposed VME64 specification allows 64-bit address and data transfers. During these bus cycles the 32 address lines are used in conjunction with the 32 data lines to pass a 64-bit address.

Interrupt handlers use A01-A03 to broadcast the level of interrupt being acknowledged during interrupt acknowledge cycles.

A01-A31 are standard three-state class signals.

1.2.7.4 AS*

Address strobe AS* is driven by masters and interrupt handlers. When asserted, it indicates that a valid address and address modifier have been placed onto the bus. The signal also qualifies other signals such as IACK*. AS* is a high current three-state signal.

1.2.7.5 BBSY*

Bus busy BBSY* is driven by masters and interrupt handlers when they are using the bus. The arbiter monitors this signal to determine when it should grant the bus to another master or interrupt handler. BBSY* is an open-collector class signal.

1.2.7.6 BCLR*

Bus clear BCLR* is driven by the bus arbiter. When asserted it informs the current master or interrupt handler that another module is requesting the bus. The conditions under which it is asserted depend upon the arbitration method being used (see Chapter 3). BCLR* is a high current totem-pole class signal.

1.2.7.7 BERR*

Bus error BERR* is driven by slave or bus timer modules. A slave asserts BERR* if an error has occurred during the bus cycle. The bus timer asserts it when the bus has locked-up. BERR* is an open-collector class signal.

1.2.7.8 BG0IN* - BG3IN* / BG0OUT* - BG3OUT*

The signals BG0IN* - BG3IN* and BG0OUT* - BG3OUT* are part of the bus grant daisy-chain and are driven by arbiters and bus requesters. The slot 01 arbiter asserts a bus grant in response to a bus request on the same level (BR0* - BR3*). The bus grant daisy-chain starts at the slot 01 system controller and propagates from module to module until the requester that initially needed the bus receives it. Each VMEbus module has a bus grant input and a bus grant output. They are standard totem-pole class signals.

1.2.7.9 BR0* - BR3*

Bus requests BR0* - BR3* are asserted by a requester whenever its master or interrupt handler needs the bus. Before accepting the bus, the master waits until the arbiter grants the bus by way of the bus grant daisy-chain BG0IN* - BG3IN*. BR0* - BR3* are open-collector class signals.

1.2.7.10 D00-D31

Data bus D00-D31 is driven by masters, slaves or interrupters. These are bidirectional signals and are used for data transfers. Different portions of the data bus are used depending upon the state of DS0*, DS1*, A01 and LWORD*. D00 - D31 are standard three-state signals.

The proposed VME64 specification allows the data bus to be used to transfer 64-bit addresses as well.

1.2.7.11 DS0*-DS1*

Data strobes DS0* and DS1* are driven by masters and interrupt handlers. These signals serve not only to qualify data, but also to indicate the size and position of the data transfer.

When combined with LWORD* and A01, the data strobes indicate the size and type of data transfer. DS0* - DS1* are high current three-state class signals.

1.2.7.12 DTACK*

Data transfer acknowledge DTACK* is driven by slaves or interrupters. During write cycles DTACK* is asserted after a slave has latched the data on the data bus. During read and interrupt acknowledge cycles, DTACK* is asserted after valid data is placed onto the data bus. DTACK* is an open-collector class signal.

1.2.7.13 GND

Ground GND is used both as a signal reference and a power return path.

1.2.7.14 IACK*

Interrupt acknowledge IACK* is driven by interrupt handlers in response to interrupt requests. It is connected to IACKIN* at slot 01 (on the backplane), and used by the IACK* daisy-chain driver to start propagation IACKIN* - IACKOUT daisy-chain. IACK* can be either an open-collector or a standard three-state class signal.

1.2.7.15 IACKIN*-IACKOUT*

The interrupt acknowledge daisy-chain IACKIN* - IACKOUT* is driven by the IACK* daisy-chain driver. These signals are used both to indicate that an interrupt acknowledge cycle is in progress and to determine which interrupters should return a STATUS/ID. They are standard totem-pole class signals.

1.2.7.16 IRQ1*-IRQ7*

Priority interrupt requests IRQ1*-IRQ7* are asserted by interrupters. Level seven is the highest priority and level one the lowest. They are open-collector class signals.

1.2.7.17 LWORD*

Long word LWORD* is driven by masters. It is used in conjunction with A01, DS0* and DS1* to indicate the size of the current data transfer. LWORD* is a standard three-state class signal.

During 64-bit data transfers (allowed under the proposed VME64 specification), LWORD* doubles as data bit D32.

1.2.7.18 RESERVED

Under VMEbus Revisions A, B, C, C.1, IEC821 and IEEE-1014-1987 the RESERVED pin was saved for future use, and not permitted to be used for any purpose. It was required to be bussed and terminated. Under the proposed VME64 specification, however, it was renamed the RETRY* pin.

1.2.7.19 RETRY*

The proposed VME64 Specification designates the (former) RESERVED pin on the P2 connector (P2-B3) as a RETRY* signal. RETRY*, together with BERR*, can be asserted by slaves to indicate that a requested data transfer cannot take place, but should be attempted again by the master in a future bus cycle. The retry provision was made to prevent deadlock (deadly embrace) conditions in bus-to-bus links and secondary buses. RETRY* is a standard three-state signal.

1.2.7.20 SERCLK-SERDAT*

The serial clock (SERCLK) and serial data (SERDAT*) signals are used for VMSbus. VMSbus is a serial bus used as an alternate data path between bus modules or subracks.

Under the proposed VME64 specification the SERCLK and SERDAT* pins were changed to user defined pins. As user defined pins, however, they can still be used for the VMSbus serial bus.

1.2.7.21 SYSCLK

16 Mhz utility clock SYSCLK is driven by the slot 01 system controller. This clock can be used for any purpose and has no timing relationship to other VMEbus signals. SYSCLK* is a high current totem-pole class signal.

1.2.7.22 SYSFAIL*

System fail SYSFAIL* can be asserted or monitored by any module and indicates that a failure has occurred in the system. The cause and the response to the failure is user defined, and its use is optional. SYSFAIL* is an open-collector class signal.

1.2.7.23 SYSRESET*

System reset SYSRESET* can be driven by any module and indicates that a reset (such as power-up) is in progress. SYSRESET* is an open-collector class signal.

1.2.7.24 WRITE*

WRITE*, the read/write signal, is driven by masters and indicates the direction of data transfer over the bus. It is asserted during a write cycle and negated during a read. WRITE* is a standard three-state class signal.

1.2.7.25 +5 STDBY

+5 STDBY is the +5 VDC standby power supply. Its use is optional.

1.2.7.26 +5 VDC, +12 VDC, -12 VDC

Three system power supplies are used. These are +5 VDC, +12 VDC and -12 VDC.

1.3 Bus Options and Mnemonics

VMEbus offers many interface options. Mnemonic symbols have been defined to describe these options. When integrating a VMEbus system, use these mnemonics to insure that all of the boards in the system will work together reliably.

1.3.1 Options

When selecting modules make sure that the options on each module are compatible with all others in the system. For example, D08(EO), D16, D32 and RMW all specify possible types of data transfer cycles that a master can generate. There are other options that might not be used. In this case its bus interface options would be described as:

D08(EO):D16:D32:RMW

The user must be aware that slave modules in a system with this master may or may not be capable of handling all of its cycle types. For example, consider a slave with the following options:

D08(EO):D16:RMW

If the master generates D08(EO), D16 or RMW bus cycles this slave would accept them. If the master generates a D32 cycle the slave would be incapable of handling it. This is not to say that the slave couldn't be used in the system, but rather the user has to insure that the master does not generate a D32 cycle to that particular slave.

1.3.2 Mnemonics

1.3.2.1 ADO

Bus modules with ADO [ADdress Only] capability can generate or accept address-only cycles. The address-only cycle can speed up a system by allowing slave and master memory decoding to happen at the same time.