

Address offset (hex)	Description
80	Enable input
0	Delay value for PTI1
4	Delay value for PTI2
8	Delay value for PTI3
c	Delay value for PTI4
10	Delay value for PTI5
14	Delay value for TS
18	Delay value for VS
a4	Delay value for Beam signal
1c	Downscale value for PTI1
20	Downscale value for PTI2
24	Downscale value for PTI3
28	Downscale value for PTI4
2c	Downscale value for PTI5
30	Downscale value for TS
34	Downscale value for VS
38	Downscale value for local clock
3c	Width value for PTI1
40	Width value for PTI2
44	Width value for PTI3
48	Width value for PTI4
4c	Width value for PTI5
50	Width value for TS
54	Width value for VS
a8	Width value for Beam signal
58	OR on/off
5c	MUX 1 selection
60	MUX 2 selection
64	Scaler register PTI1 (read only)
68	Scaler register PTI2 (read only)
6c	Scaler register PTI3 (read only)
70	Scaler register PTI4 (read only)
74	Scaler register PTI5 (read only)
78	Scaler register TS (read only)
7c	Scaler register VS (read only)
8c	Scaler reset
b4	Scaler register Dead time (read only)
90	Enable MDC/TOF branch + Width value for MCD_TOF_out
94	Scaler channel selection for TOF and MDC
98	Scaler register for MDC (read only)
9c	Scaler register for TOF (read only)
84	Width for GT (output)

a0	PTI5 (mux2) and TS (mux1) alternate input
a4	High voltage inhibit dealy
a8	High voltage internal inhibit width
ac	High voltage external inhibit width
b0	Disable TS gating
b8	Scaler register PTI1 accepted (read only)
bc	Scaler register PTI2 accepted (read only)
c0	Scaler register PTI3 accepted (read only)
c4	Scaler register PTI4 accepted (read only)
c8	Scaler register PTI5 accepted (read only)
cc	Scaler register TS accepted (read only)
d0	Scaler register VS accepted (read only)
d4	Scaler register MUX 1 (read only)
d8	Scaler register MUX 2 (read only)
dc	Calibration trigger disable
88	Communication bus enable (TRB + DTU)
e0	DTU error