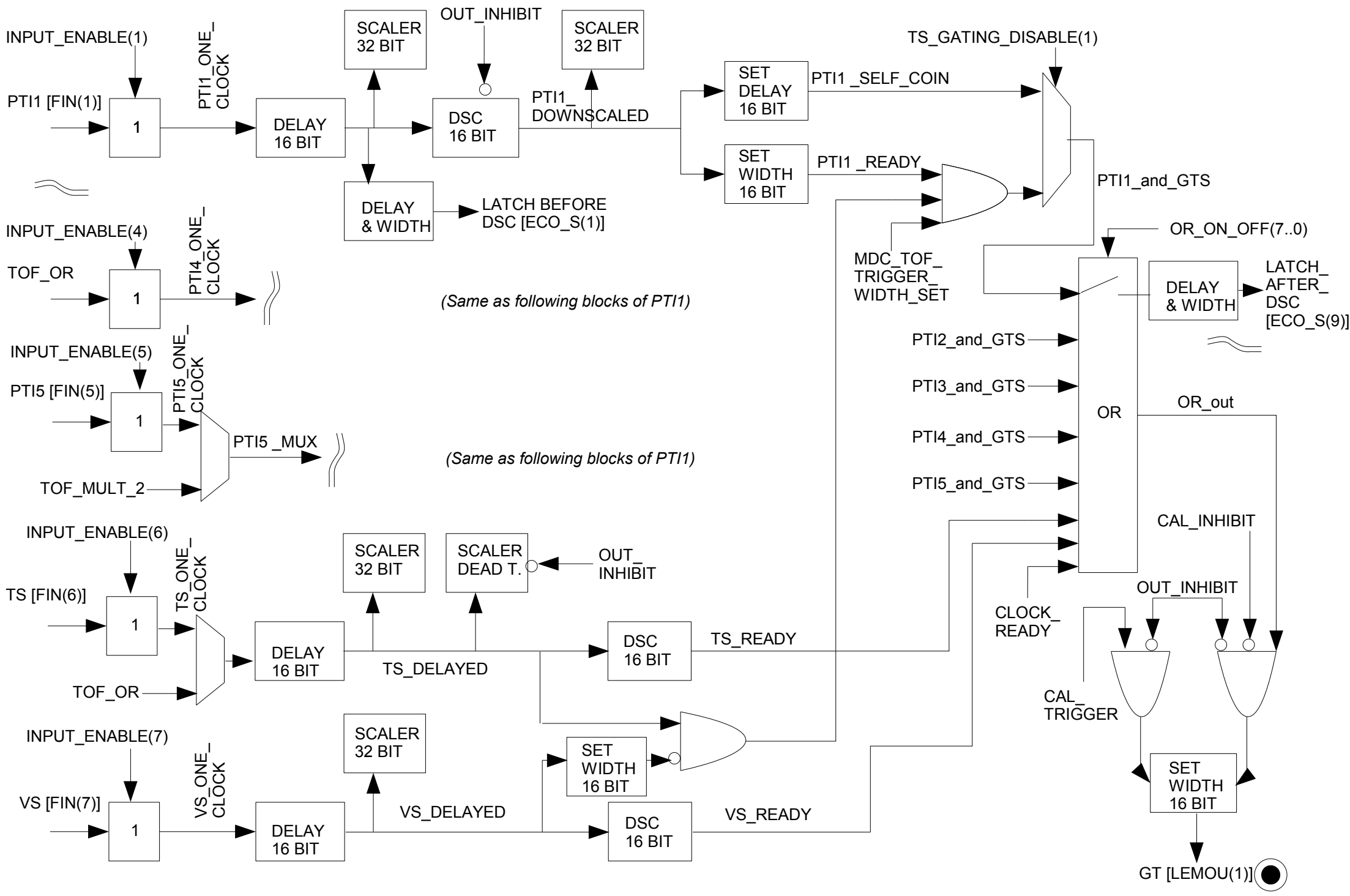
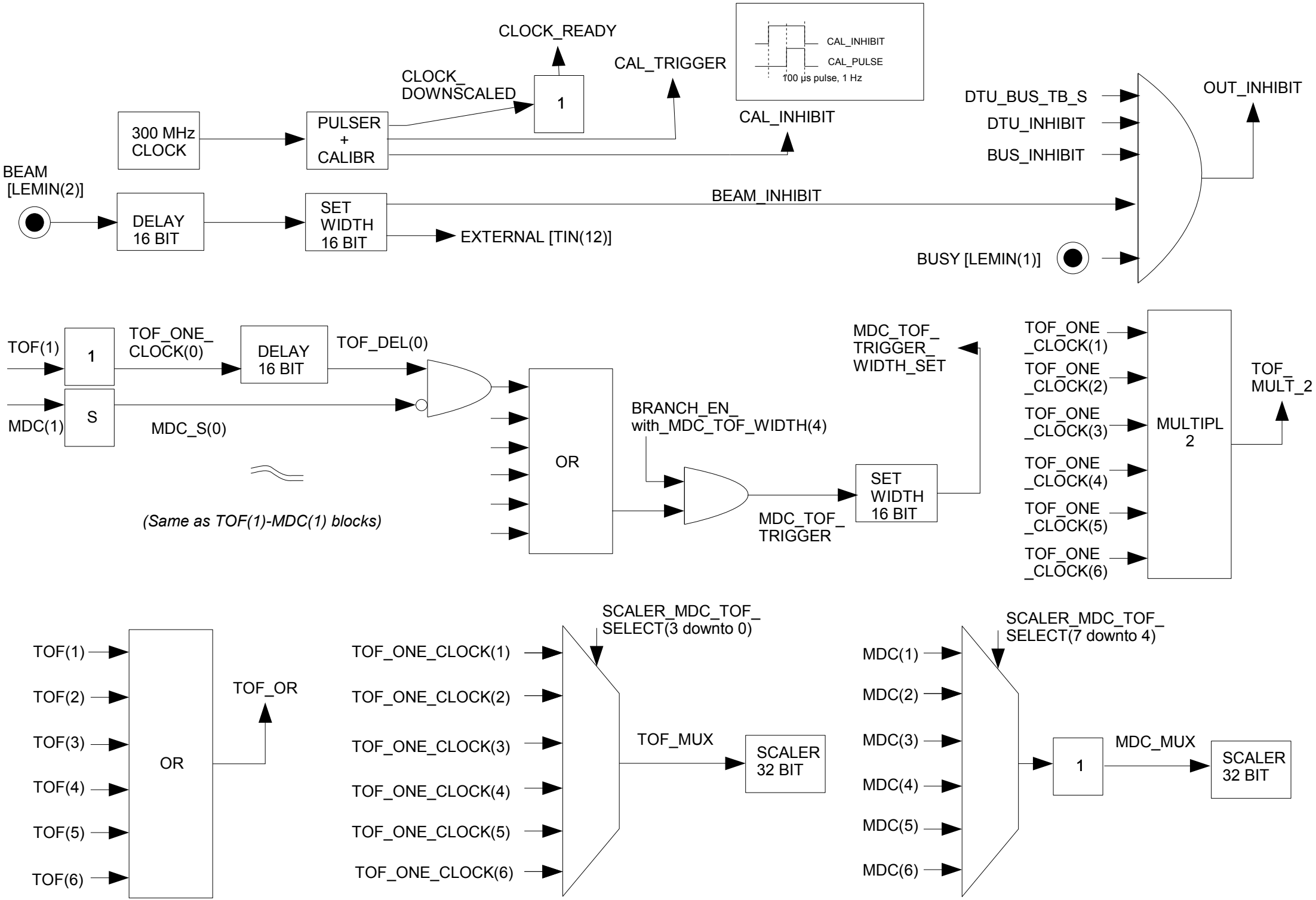

INPUT_ENABLE(1)
PTI1 [FIN(1)]
1
PTI1_ONE_ CLOCK
DELAY 16 BIT
SCALER 32 BIT
OUT_INHIBIT
DSC 16 BIT
SCALER 32 BIT
PTI1_ DOWNSCALED
DELAY & WIDTH
LATCH BEFORE DSC [ECO_S(1)]
SET DELAY 16 BIT
PTI1 _SELF_COIN
SET WIDTH 16 BIT
PTI1 _READY
TS_GATING_DISABLE(1)
PTI1_and_GTS
MDC_TOF_ TRIGGER_ WIDTH_SET
OR_ON_OFF(7..0)
DELAY & WIDTH
LATCH_ AFTER_ DSC [ECO_S(9)]
INPUT_ENABLE(4)
TOF_OR
1
PTI4_ONE_ CLOCK
(Same as following blocks of PTI1)
INPUT_ENABLE(5)
PTI5 [FIN(5)]
1
PTI5_ONE_ CLOCK
PTI5 _MUX
TOF_MULT_2
(Same as following blocks of PTI1)
PTI2_and_GTS
PTI3_and_GTS
PTI4_and_GTS
PTI5_and_GTS
OR
OR_out
CAL_INHIBIT
INPUT_ENABLE(6)
TS [FIN(6)]
1
TS_ONE_ CLOCK
TOF_OR
SCALER 32 BIT
SCALER DEAD T.
OUT_ INHIBIT
DELAY 16 BIT
TS_DELAYED
DSC 16 BIT
TS_READY
CLOCK_ READY
OUT_INHIBIT
CAL_ TRIGGER
INPUT_ENABLE(7)
VS [FIN(7)]
1
VS_ONE_ CLOCK
DELAY 16 BIT
SCALER 32 BIT
VS_DELAYED
SET WIDTH 16 BIT
DSC 16 BIT
VS_READY
SET WIDTH 16 BIT
GT [LEMOU(1)]


CLOCK_READY
CAL_TRIGGER
CAL_INHIBIT
CAL_PULSE
100 µs pulse, 1 Hz
CLOCK_
DOWNSCALED
1
300 MHz
CLOCK
PULSER
+
CALIBR
CAL_INHIBIT
DTU_BUS_TB_S
DTU_INHIBIT
BUS_INHIBIT
OUT_INHIBIT
BEAM
[LEMIN(2)]
DELAY
16 BIT
SET
WIDTH
16 BIT
BEAM_INHIBIT
EXTERNAL [TIN(12)]
BUSY [LEMIN(1)]
TOF(1)
1
TOF_ONE_
CLOCK(0)
DELAY
16 BIT
TOF_DEL(0)
MDC(1)
S
MDC_S(0)
(Same as TOF(1)-MDC(1) blocks)
OR
BRANCH_EN_
with_MDC_TOF_WIDTH(4)
MDC_TOF_
TRIGGER
SET
WIDTH
16 BIT
MDC_TOF_
TRIGGER_
WIDTH_SET
TOF_ONE
_CLOCK(1)
TOF_ONE
_CLOCK(2)
TOF_ONE
_CLOCK(3)
TOF_ONE
_CLOCK(4)
TOF_ONE
_CLOCK(5)
TOF_ONE
_CLOCK(6)
MULTIPL
2
TOF_
MULT_2
TOF(1)
TOF(2)
TOF(3)
TOF(4)
TOF(5)
TOF(6)
OR
TOF_OR
SCALER_MDC_TOF_
SELECT(3 downto 0)
TOF_ONE_CLOCK(1)
TOF_ONE_CLOCK(2)
TOF_ONE_CLOCK(3)
TOF_ONE_CLOCK(4)
TOF_ONE_CLOCK(5)
TOF_ONE_CLOCK(6)
TOF_MUX
SCALER
32 BIT
SCALER_MDC_TOF_
SELECT(7 downto 4)
MDC(1)
MDC(2)
MDC(3)
MDC(4)
MDC(5)
MDC(6)
1
MDC_MUX
SCALER
32 BIT