Level 1 trigger processing by VULOM3 board *

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A new HADES Level 1 triggerbox has been implemented using the programmable logic included in a VULOM3 (VME Universal LOgic Module) module. This development will reduce beam time losses caused by the problematic maintenance of the old Level 1 trigger, bringing at the same time better control and monitor capabilities [1].

Firmware architecture

The Level 1 triggerbox collects signals from several HADES detectors, remarkably the upstream diamond detector (Timing Signal), multiplicity in TOF detectors (Physic Triggers) and downstream diamond detector (Veto Signal). The selection process is quite straightforward: every PT pulse enables an acceptance time slot, if a received TS pulse falls inside the time slot and it is not inhibited by VS then an output trigger pulse is issued.

The VULOM3 is an extremely flexible VME module offering up to 32 ECL inputs, 32 ECL outputs and 4 LEMO selectable TTL or NIM connectors. It is equipped with a Xilinx VirtexIV FPGA, on-board SRAM and FLASH memory capable of retaining up to 8 different configurations, making it possible to use the module in a stand-alone setup with an instant-up feature.

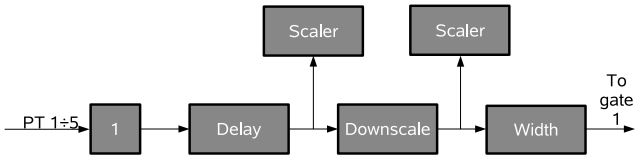

Figure 1: Physic trigger chain block diagram

The firmware architecture is organized into three slightly different chains. The PT chain consists of the following blocks: a sampler, a selectable delay (0-50 ns in 3.3 ns steps), a selectable downscale (up to 2^{16} in power of 2 steps) and a selectable width (3-53 ns in 3.3 ns steps). The delay and width blocks are used to tune the correct timing between PT and TS; in addition there are two 32-bit scalers, before and after the downscale, to provide adequate counting rate capability. A 300 MHz clock is used to synchronize the whole chain: in this application the output jitter is solely determined by the clock period and such a high frequency was chosen to minimize it. The other two chains also have a similar structure: the TS path lacks the downscale and width blocks, the VS path lacks only the downscale block.

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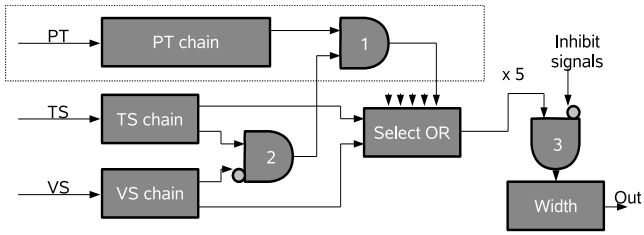

Figure 2: Triggerbox block diagram

A TS pulse entering the triggerbox passes trough the TS chain and arrives to gate 2. Here it can be inhibited by VS, otherwise it proceeds to gate 1. Meanwhile, one or more PT move through the PT chain and stop at gate 1. The TS is used to gate the five PT, and the resulting signals are selectively ORed. After that the output must cross gate 3, where it can be inhibited, and finally exits through a fixed width block. The inhibit signal at gate 3 is obtained from three different sources: a LEMO input, an internal calibration inhibit pulse (1 Hz, 200 µs width) and a high voltage inhibit pulse (spill trigger) with programmable delay and width (0-25 s in 0.1 s steps).

For every trigger issued by the VULOM3 an event packet containing trigger tag and code, latch-state and scaler values is built and sent to the TRB[3] via a dedicated bus. In addition, for the sake of mantaining compatibility with the existing machinery, the triggerbox is equipped with a CTU/DTU trigger bus (replacing the CTU module [2]) and is able to send latch-information as well. Other features include a programmable output pulser (2 MHz - 70 Hz) for testing DAQ, the possibility to create TS on board using a ORed TOF-signal, a sectorwise MDC/TOF coincidence and two multiplexed outputs for timing adjust purposes. Every parameter register can be conveniently set and monitored using the graphical EPICS interface.

The VULOM3 board was successfully tested in October 2007 beam time and it will replace the old triggerbox in the upcoming beam times.

References

[1] J. Hoffman; VULOM3, VME Universal Logic Module, Version 3
http://www.gsi.de/onTEAM/grafik/1130845854/vulom3.pdf

[2] E. Lins; Detector Trigger Unit Technical Manual, HADES-Wiki

[3] M. Traxler, A General Purpose Trigger and Readout Board (TRB) for HADES and FAIR-Experiments, GSI Scientific Report (2006)